MYP018CNE3

-30V P-Channel Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

The MYP018CNE3 is the single P-Channel logic enhancement mode power field effect transistors to provide excellent $R_{DS(on)}$, low gate charge and low gate resistance.

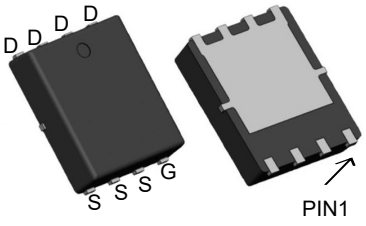
RoHS Compliant

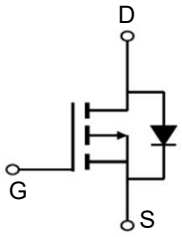
Features

V_{DSS}	-30	V
I_D	-30	A
$R_{DS(ON)}$(atV_{GS} =-10V)	12.5	mÝ
$R_{DS(ON)}$(atV_{GS} =-4.5V)	22	mÝ

Application

- Battery protection System
- Switching power supply, SMPS
- DC/DC Converter
- DC/AC Converter
- Load Switch





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MYP018CNE3	PDFN3*3-8L	018DPE	5000

Absolute Maximum Ratings (T_J=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain- Source Voltage	-30	V
VGS	Gate- Source Voltage	±20	V
I_D@T_A=25℃	Drain Current[3] , V_{GS} @ 10V	-30	A
I_D@T_A=70℃	Drain Current[3] , V_{GS} @ 10V	-23	A
IDM	Pulsed Drain Current[1]	-80	A
P_D@T_A=25℃	Total Power Dissipation	3.57	W
TSTG	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃
Rthj-c	Maximum Thermal Resistance, Junction- case	6	℃/W
Rthj-a	Maximum Thermal Resistance, Junction- ambient[3]	35	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30	-	-	V
RDS(ON)	Static Drain-Source On-Resistance[2]	V_{GS}=- 10V, I_D=-20A	-	12.5	15	mΩ
		V_{GS}=-4.5V, I_D=- 10A	-	22	26	mΩ
VGS(th)	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.2	-1.6	-2.0	V
g_{fs}	Forward Transconductance	V_{DS}=- 10V, I_D=-6A	-	15	-	S
IDSS	Drain-Source Leakage Current	V_{DS}=-30V, V_{GS}=0V	-	-	-1	uA
IGSS	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge	I_D=-6A V_{DS}=- 15V V_{GS}=-4.5V	-	15	24	nC
Q_{gs}	Gate-Source Charge		-	3	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge		-	8	-	nC
td(on)	Turn-on Delay Time	V_{DS}=- 15V I_D=- 1A R_G=3.3Ω V_{GS}=- 10V	-	12	-	ns
t_r	Rise Time		-	7.5	-	ns
td(off)	Turn-off Delay Time		-	39	-	ns
t_f	Fall Time		-	21	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=- 15V f=1.0MHz. I_S=-6A, V_{GS}=0V, dI/dt=100A/μs	-	1260	2000	pF
Coss	Output Capacitance		-	245	-	pF
C_{rss}	Reverse Transfer Capacitance		-	210	-	pF
trr	Reverse Recovery Time		-	19	-	ns
Q_{rr}	Reverse Recovery Charge		-	10	-	nC

Notes:
1.Pulse width limited by Max. junction temperature.
2.Pulse test

Typical Characteristics

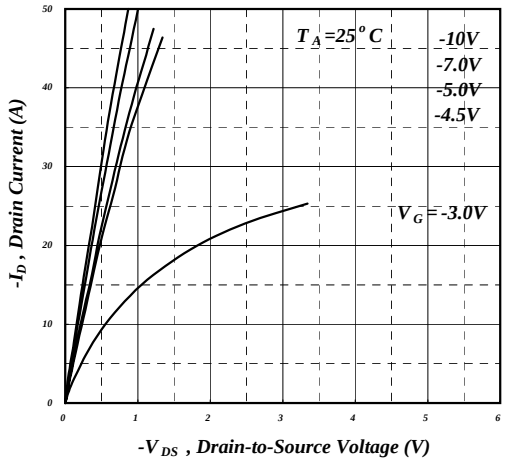


Fig 1. Typical Output Characteristics

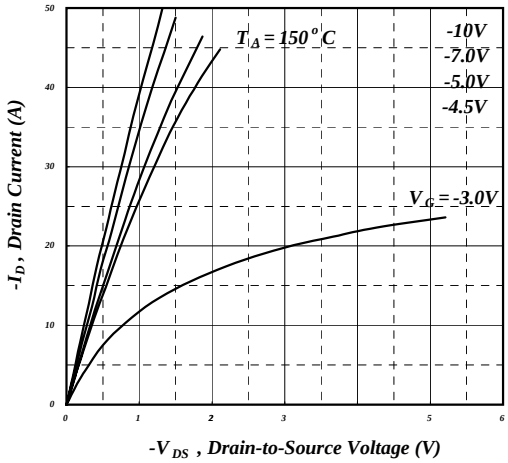


Fig 2. Typical Output Characteristics

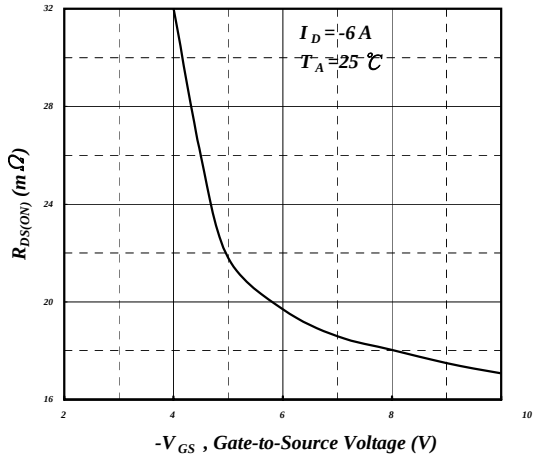


Fig 3. On-Resistance v.s. Gate Voltage

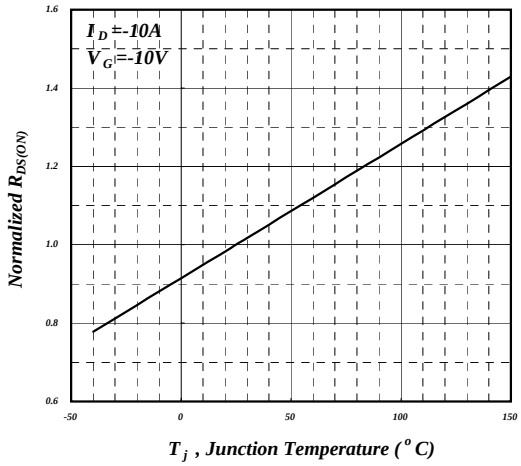


Fig 4. Normalized On-Resistance v.s. Junction Temperature

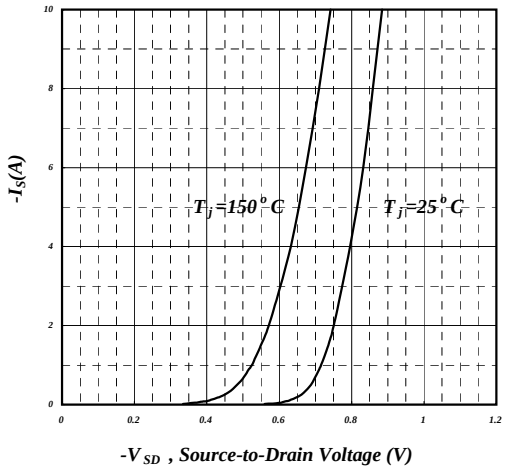


Fig 5. Forward Characteristic of Reverse Diode

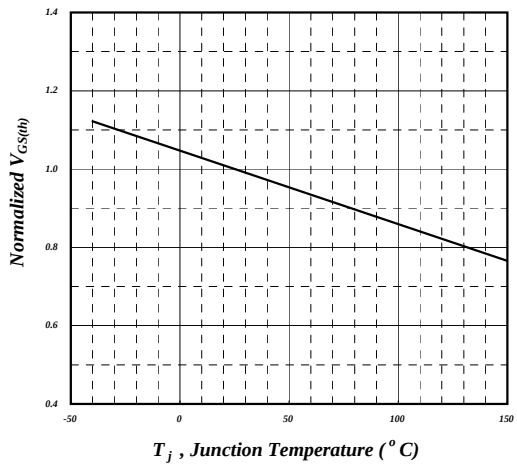


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

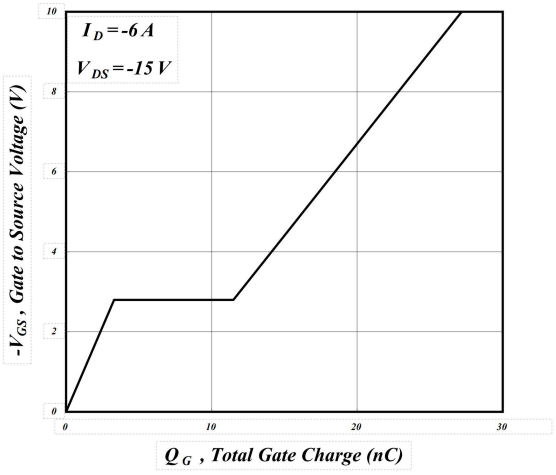


Fig 7. Gate Charge Characteristics

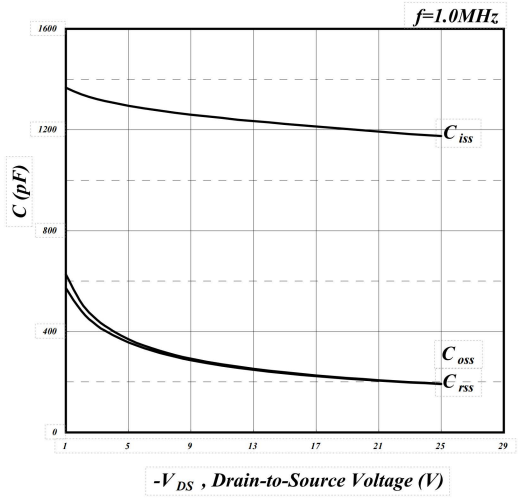


Fig 8. Typical Capacitance Characteristics

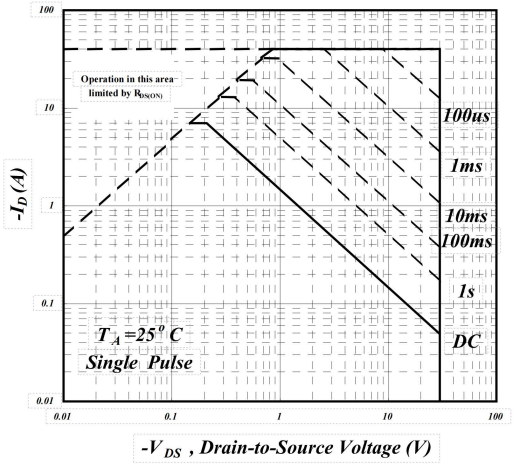


Fig 9. Maximum Safe Operating Area

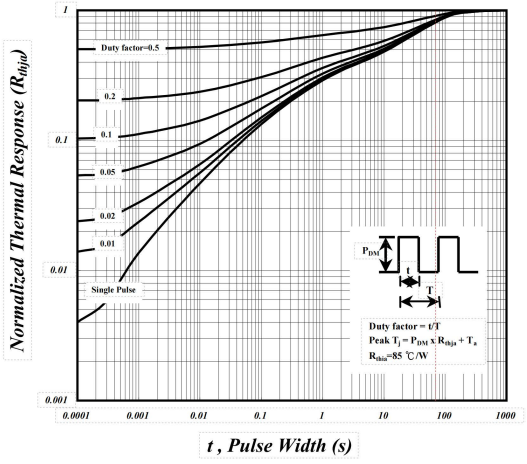


Fig 10. Effective Transient Thermal Impedance

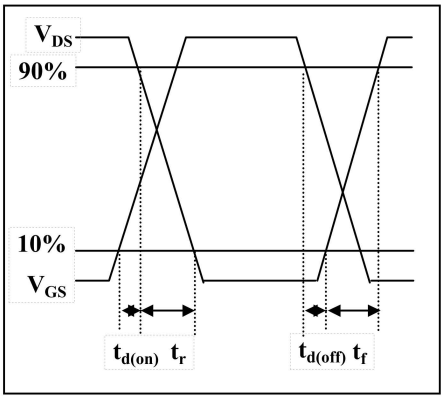


Fig 11. Switching Time Waveform

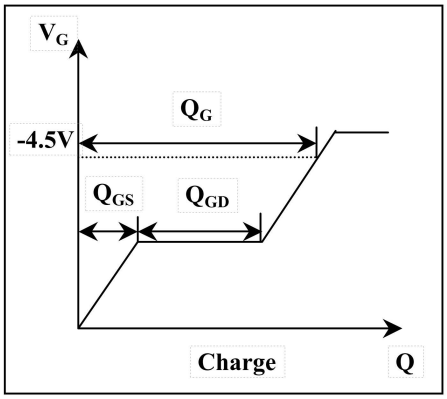
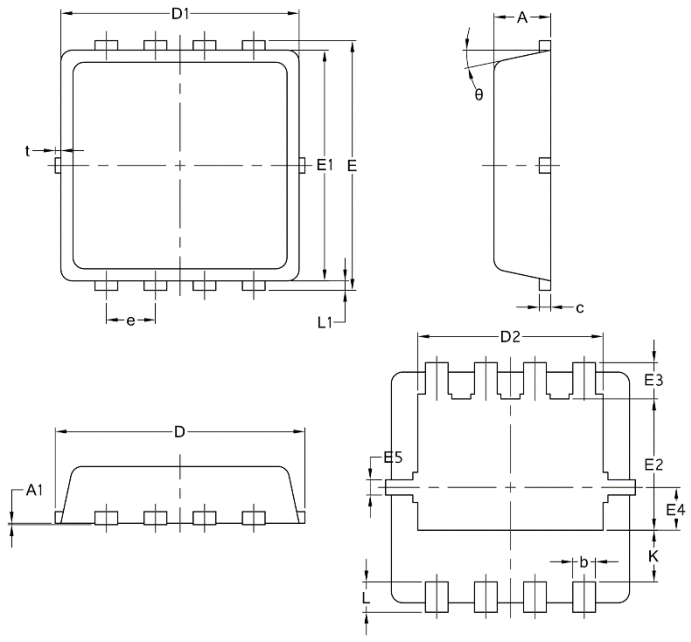


Fig 12. Gate Charge Waveform

Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14