

## General Description

The MY85N12NE5 use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching. This device is specially designed to get better ruggedness and suitable to use in

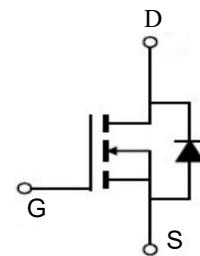
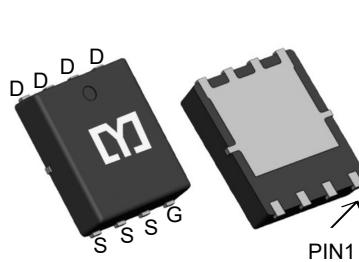


## Features

X <sub>FUU</sub>	120	X
K <sub>F</sub>	85	C
T <sub>FUQP+CVXI U? 10X+</sub>	>10	o á
T <sub>FUQP+CVXI U? 4.5X+</sub>	>13	o á

## Application

- Power supply Motor control
- Synchronous-rectification Isolated DC
- Synchronous-rectification applications



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY85N12NE5	PDFN5*6-8L	8512DN	5000

## Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain source voltage	V <sub>DS</sub>	120	V
Gate source voltage	V <sub>GS</sub>	±20	V
Continuous drain current <sup>1)</sup> , $T_C=25^\circ\text{C}$	I <sub>D</sub>	85	A
Pulsed drain current <sup>2)</sup> , $T_C=25^\circ\text{C}$	I <sub>D</sub> , pulse	150	A
Power dissipation <sup>3)</sup> , $T_C=25^\circ\text{C}$	P <sub>D</sub>	140	W
Single pulsed avalanche energy <sup>4)</sup>	E <sub>AS</sub>	53.8	mJ
Operation and storage temperature	T <sub>stg</sub> , T <sub>j</sub>	-55 to 150	°C
Thermal resistance, junction-case	R <sub>θJC</sub>	0.89	°C/W
Thermal resistance, junction-ambient <sup>5)</sup>	R <sub>θJA</sub>	62	°C/W

**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Parameter	Symbol	Min	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	$V_{BDSS}$	120		200	V	$V_{GS}=0\text{ V}$ , $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(\text{th})}$	1.5		2.5	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		8.0	10	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$
Drain-source on-state resistance	$R_{DS(\text{ON})}$		11.0	13.0	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$ , $I_D=20\text{ A}$
Gate-source leakage current	$I_{GSS}$			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	$I_{DSS}$			1	$\text{uA}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$
Input capacitance	$C_{iss}$		2640.1		$\text{pF}$	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=100\text{ kHz}$
Reverse transfer capacitance	$C_{rss}$		11.2		$\text{pF}$	
Turn-on delay time	$t_{d(\text{on})}$		22.3		ns	$V_{GS}=10\text{ V}$ , $V_{DS}=50\text{ V}$ , $R_G=2\text{ }\Omega$ , $I_D=25\text{ A}$
Rise time	$t_r$		9.7		ns	
Turn-off delay time	$t_{d(\text{off})}$		85		ns	
Fall time	$t_f$		112.3		ns	
Total gate charge	$Q_g$		33.1		nC	
Gate-source charge	$Q_{gs}$		5.6		nC	$I_D=25\text{ A}$ , $V_{DS}=50\text{ V}$ , $V_{GS}=10\text{ V}$
Gate-drain charge	$Q_{gd}$		7.2		nC	
Gate plateau voltage	$V_{plateau}$		3.1		V	
Diode forward current	$I_s$			50	A	$V_{GS}<V_{th}$
Pulsed source current	$ISP$			150		
Diode forward voltage	$V_{SD}$			1.3	V	$I_s=12\text{ A}$ , $V_{GS}=0\text{ V}$
Reverse recovery time	$t_{rr}$		62.3		ns	$I_s=25\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$		135.3		nC	
Peak reverse recovery current	$I_{rrm}$		3.5		A	

**Note**

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3)  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.
- 4)  $V_{DD}=50\text{ V}$ ,  $R_G=50\text{ }\Omega$ ,  $L=0.3\text{ mH}$ , starting  $T_j=25^\circ\text{C}$ .
- 5) The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_a=25^\circ\text{C}$ .

### Typical Characteristics

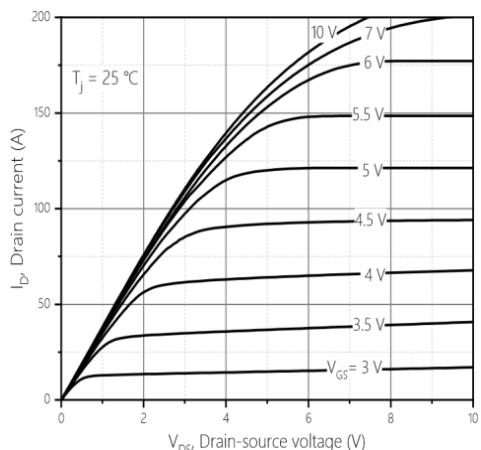


Figure 1, Typ. output characteristics

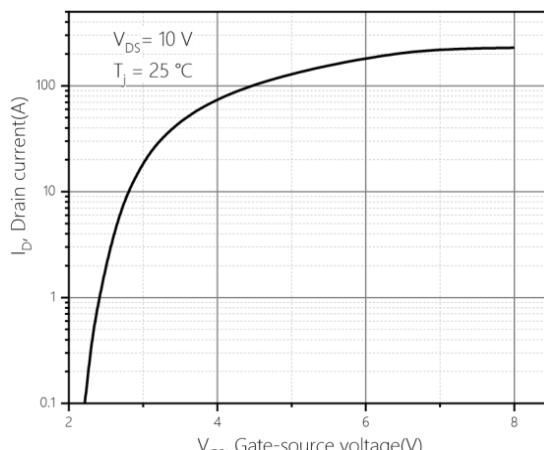


Figure 2, Typ. transfer characteristics

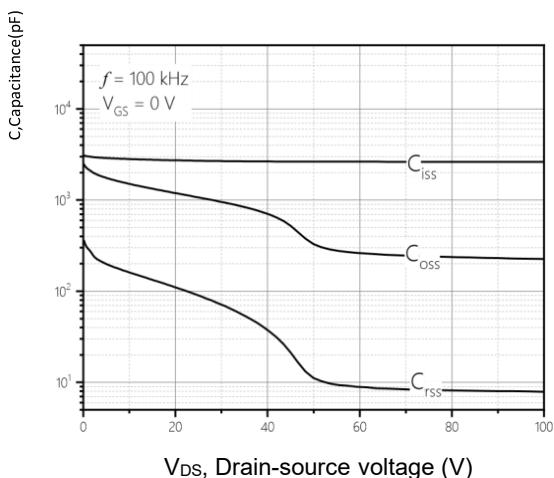


Figure 3, Typ. capacitances

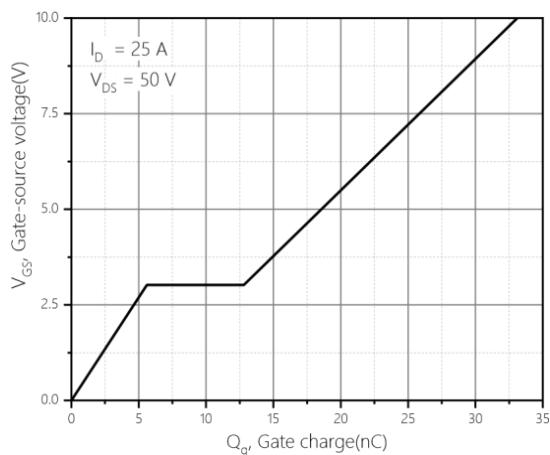


Figure 4, Typ. gate charge

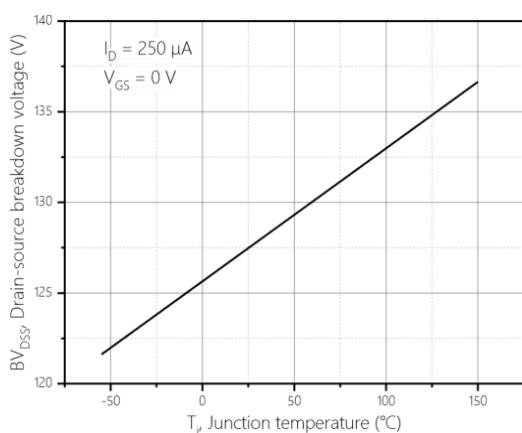


Figure 5, Drain-source breakdown voltage

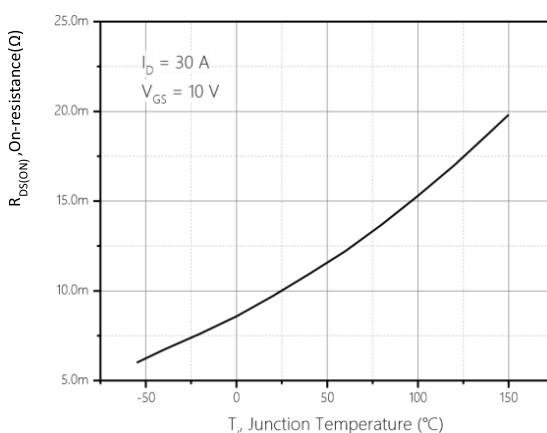


Figure 6, Drain-source on-state resistan

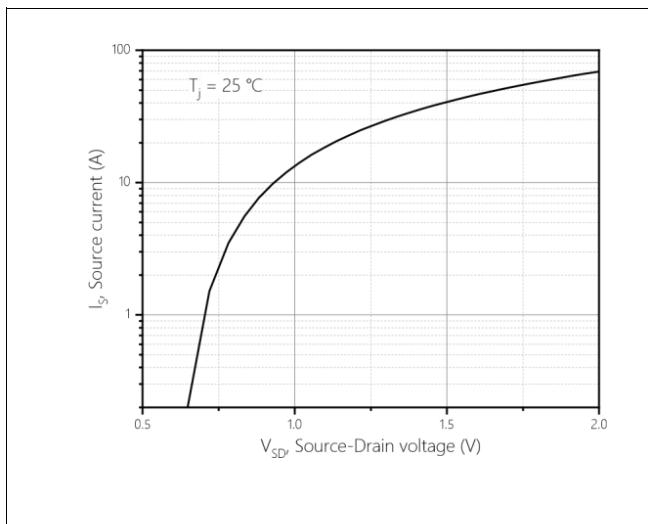


Figure 7, Forward characteristic of body diode

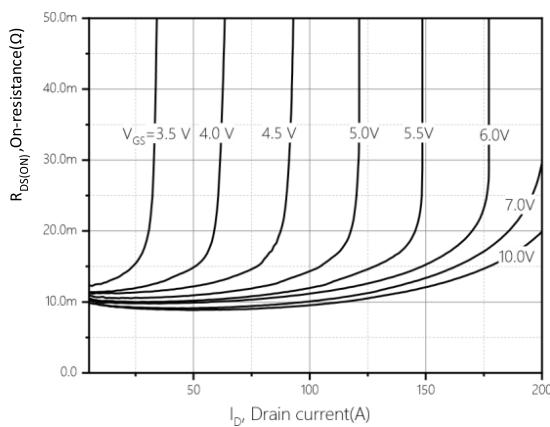


Figure 8, Drain-source on-state resistance

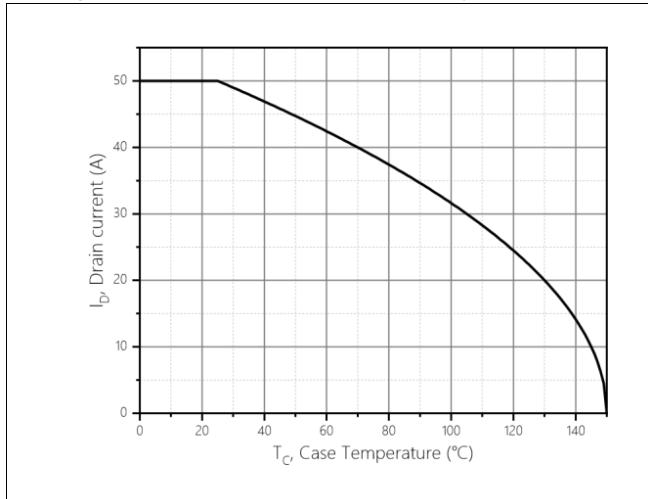


Figure 9, Drain current

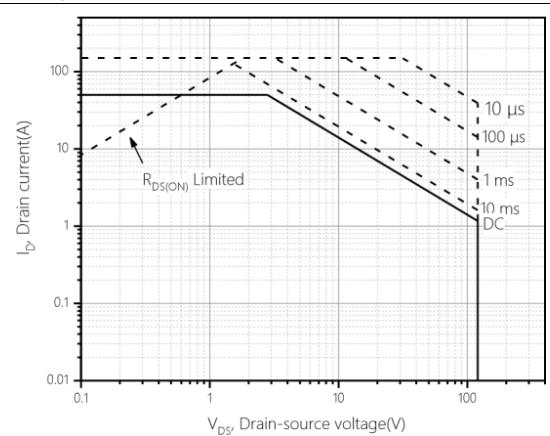


Figure 10, Safe operation area T<sub>c</sub>=25 °C

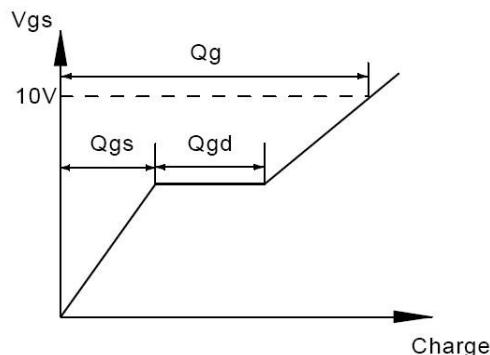
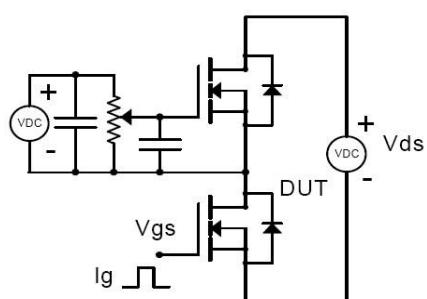


Figure 1, Gate charge test circuit &amp; waveform

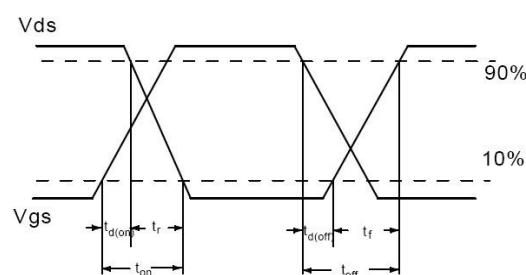
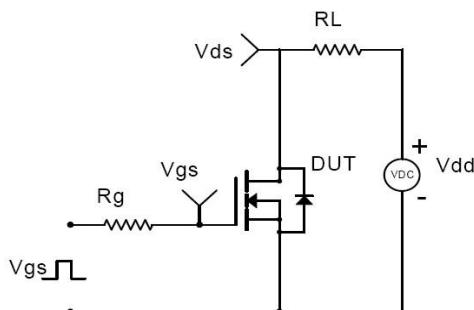


Figure 2, Switching time test circuit &amp; waveforms

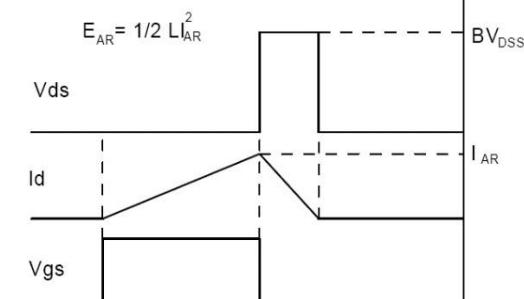
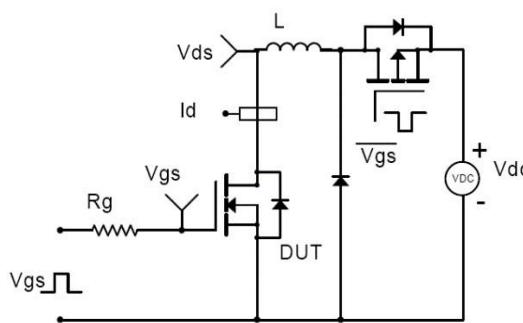
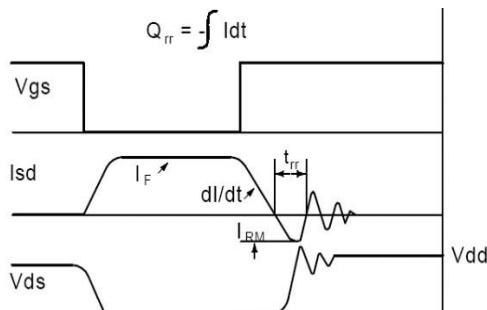
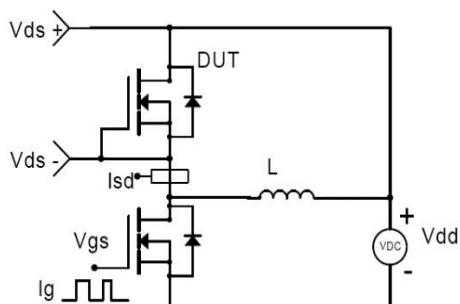
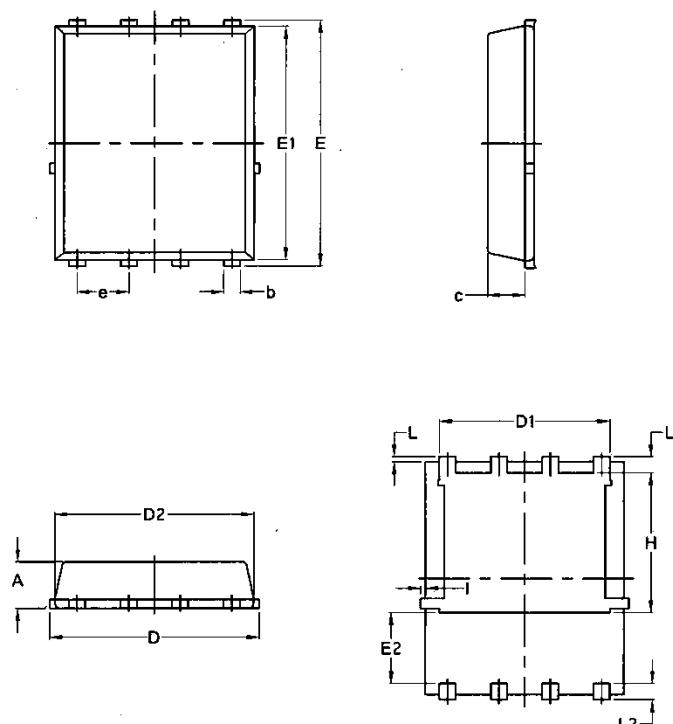


Figure 3, Unclamped inductive switching (UIS) test circuit &amp; waveforms



## Package Mechanical Data-DFN5\*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070