

## General Description

The MY65T180PT is silicon N-channel Enhanced VDMOSFETs, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

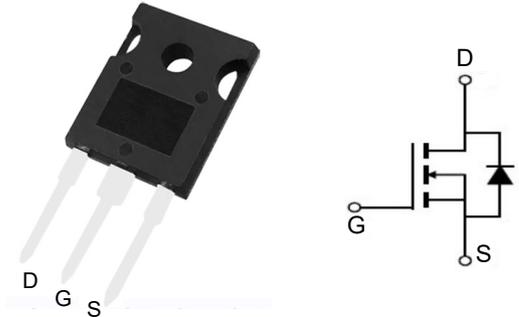


## Features

|  |      |          |
|--|------|----------|
| $V_{DSS}$                                    | 650  | V        |
| $I_D$  | 20   | A        |
| $P_D(T_C=25\text{ }^\circ\text{C})$          | 416  | W        |
| $R_{DS(ON)}(\text{at } V_{GS} = 10\text{V})$ | 0.27 | $\Omega$ |

## Application

- Fast Switching
- Low ON Resistance
- Low Gate Charge
- Power factor correction



## Package Marking and Ordering Information

| Product ID | Pack   | Marking    | Qty(PCS) |
|------------|--------|------------|----------|
| MY65T180PT | TO-247 | MY65T180PT | 600      |

## Absolute Maximum Ratings ( $T_C=25\text{ }^\circ\text{C}$ unless otherwise noted)

| Symbol          | Parameter                                       | Max.                              | Units              |
|-----------------|---|-----------------------------------|--------------------|
| $V_{DSS}$       | Drain-Source Voltage                            | 650                               | V                  |
| $V_{GSS}$       | Gate-Source Voltage                             | $\pm 30$                          | V                  |
| $I_D$           | Continuous Drain Current                        | $T_C = 25\text{ }^\circ\text{C}$  | 20                 |
|                 |   | $T_C = 100\text{ }^\circ\text{C}$ | 13                 |
| $I_{DM}$        | Pulsed Drain Current <sup>note1</sup>           | 80                                | A                  |
| $E_{AS}$        | Single Pulsed Avalanche Energy <sup>note2</sup> | 1350                              | mJ                 |
| $P_D$           | Power Dissipation                               | $T_C = 25\text{ }^\circ\text{C}$  | 416                |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case            | 0.3                               | $^\circ\text{C/W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient         | 60                                | $^\circ\text{C/W}$ |
| $T_J, T_{STG}$  | Operating and Storage Temperature Range         | -55 to +150                       | $^\circ\text{C}$   |

**Electrical Characteristics (T<sub>c</sub>=25 °C, unless otherwise noted)**

| Symbol  | Parameter  | Test Condition  | Min. | Typ. | Max. | Units |
|---|--|---|------|------|------|-------|
| <b>Off Characteristic</b>                                     |  |   |      |      |      |       |
| V <sub>(BR)DSS</sub>  | Drain-Source Breakdown Voltage                           | V <sub>GS</sub> =0V, I <sub>D</sub> =250μA                          | 650  | -    | -    | V     |
| I <sub>DSS</sub>  | Zero Gate Voltage Drain Current                          | V <sub>DS</sub> = 600V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C | -    | -    | 1    | μA    |
| I <sub>GSS</sub>  | Gate to Body Leakage Current                             | V <sub>DS</sub> =0V, V <sub>GS</sub> = ±30V                         | -    | -    | ±100 | nA    |
| <b>On Characteristics</b>                                     |  |   |      |      |      |       |
| V <sub>GS(th)</sub>   | Gate Threshold Voltage                                   | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA           | 2    | 3    | 4    | V     |
| R <sub>DS(on)</sub>   | Static Drain-Source on-Resistance note3                  | V <sub>GS</sub> =10V, I <sub>D</sub> =10A                           | -    | 0.27 | 0.45 | Ω     |
| <b>Dynamic Characteristics</b>                                |  |   |      |      |      |       |
| C <sub>iss</sub>  | Input Capacitance  | V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1.0MHz             | -    | 2980 | -    | pF    |
| C <sub>oss</sub>  | Output Capacitance                                       |   | -    | 291  | -    | pF    |
| C <sub>rss</sub>  | Reverse Transfer Capacitance                             |   | -    | 40   | -    | pF    |
| Q <sub>g</sub>  | Total Gate Charge  | V <sub>DD</sub> = 480V, I <sub>D</sub> = 20A, V <sub>GS</sub> = 10V | -    | 80   | -    | nC    |
| Q <sub>gs</sub>   | Gate-Source Charge                                       |   | -    | 12   | -    | nC    |
| Q <sub>gd</sub>   | Gate-Drain("Miller") Charge                              |   | -    | 34   | -    | nC    |
| <b>Switching Characteristics</b>                              |  |   |      |      |      |       |
| t <sub>d(on)</sub>  | Turn-on Delay Time                                       | V <sub>DD</sub> = 250V, I <sub>D</sub> =20A, R <sub>G</sub> = 25Ω   | -    | 37   | -    | ns    |
| t <sub>r</sub>  | Turn-on Rise Time  |   | -    | 66   | -    | ns    |
| t <sub>d(off)</sub>   | Turn-off Delay Time                                      |   | -    | 175  | -    | ns    |
| t <sub>f</sub>  | Turn-off Fall Time                                       |   | -    | 84   | -    | ns    |
| <b>Drain-Source Diode Characteristics and Maximum Ratings</b> |  |   |      |      |      |       |
| I <sub>S</sub>  | Maximum Continuous Drain to Source Diode Forward Current |   | -    | -    | 20   | A     |
| I <sub>SM</sub>   | Maximum Pulsed Drain to Source Diode Forward Current     |   | -    | -    | 80   | A     |
| V <sub>SD</sub>   | Drain to Source Diode Forward Voltage                    | V <sub>GS</sub> = 0V, I <sub>SD</sub> = 20A                         | -    | -    | 1.4  | V     |
| t <sub>rr</sub>   | Reverse Recovery Time                                    | V <sub>GS</sub> =0V, I <sub>S</sub> =20A, di/dt=100A/μs             | -    | 450  | -    | ns    |
| Q <sub>rr</sub>   | Reverse Recovery Charge                                  |   | -    | 7.1  | -    | μC    |

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. I<sub>AS</sub> =16A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub>= 25°C

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤1%

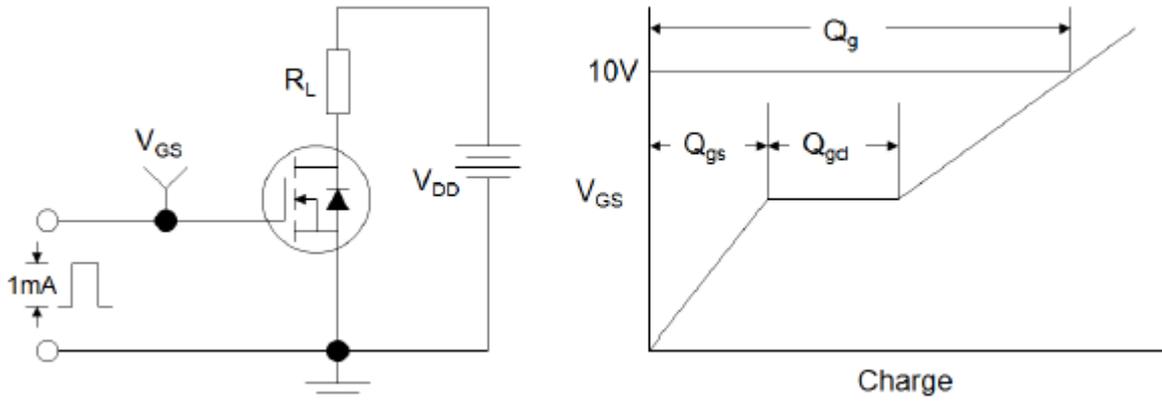


Figure1:Gate Charge Test Circuit & Waveform

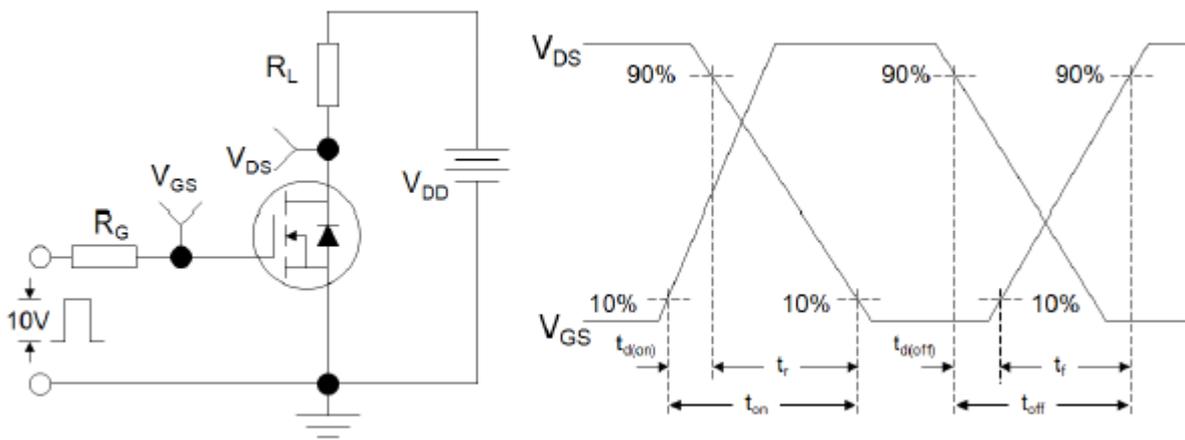


Figure 2: Resistive Switching Test Circuit & Waveforms

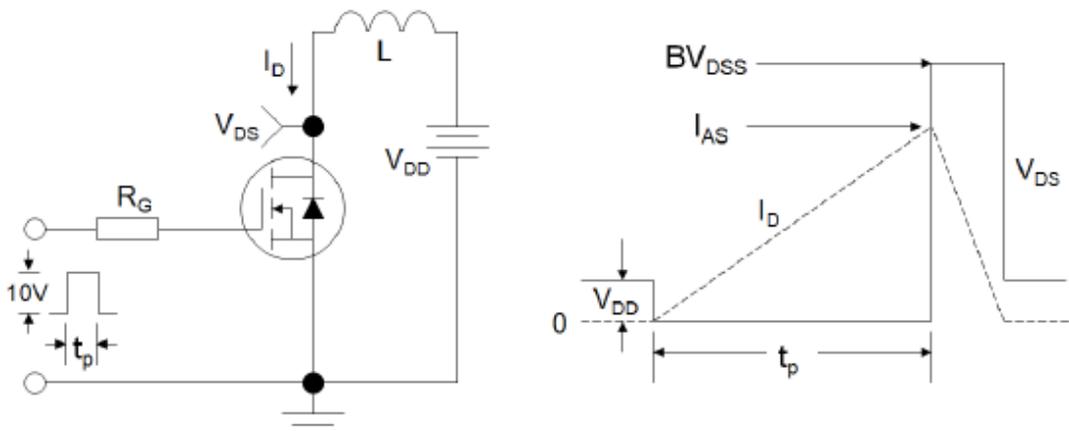
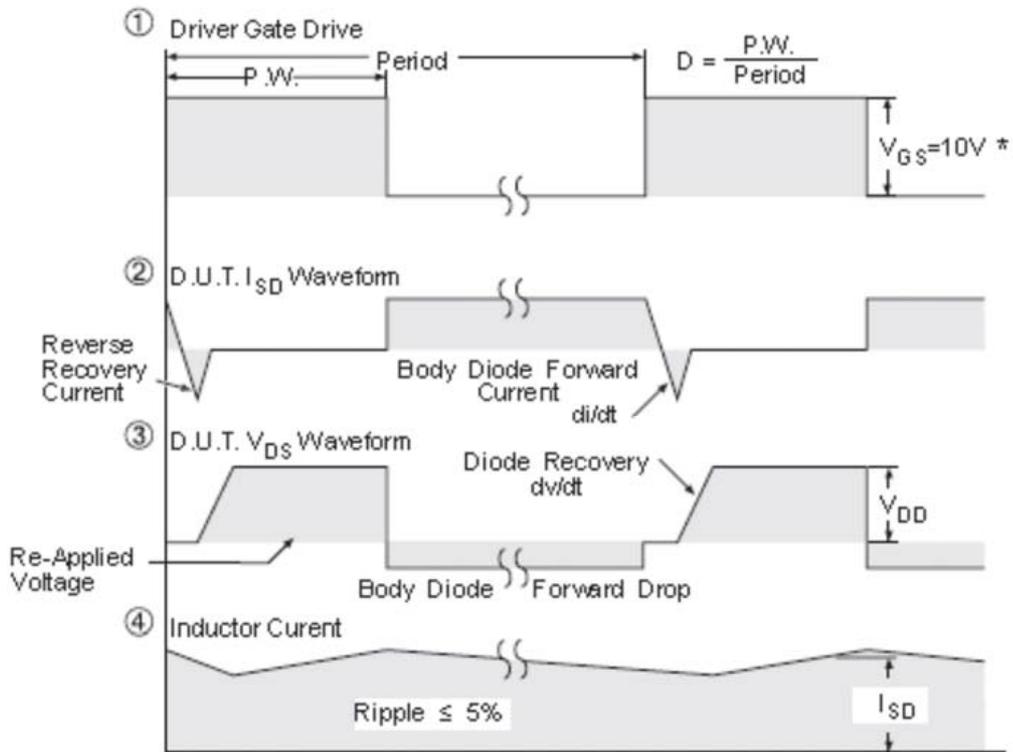
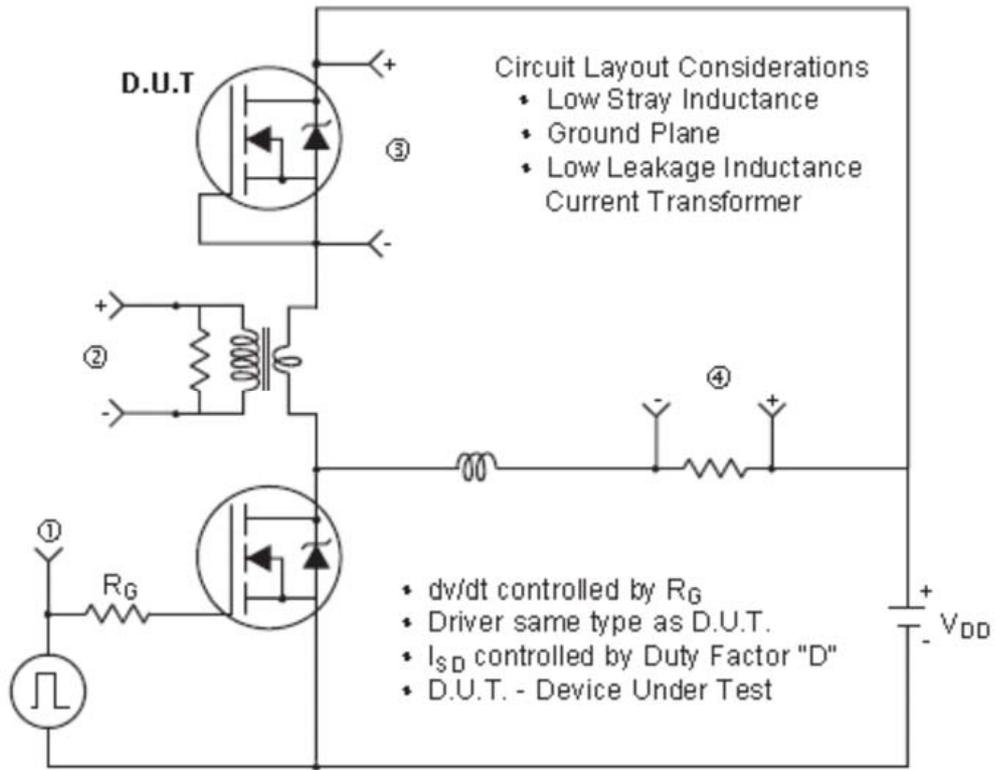


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



\*  $V_{GS} = 5V$  for Logic Level Devices

Figure 4: Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms (For N-channel)

