

General Description

The MY5N50D is silicon N-CH Enhanced VDMOSFETS is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

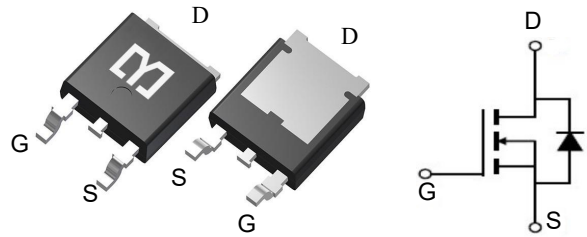


Features

V_{DSS}	500	V
I_D	5	A
$P_D(T_C=25^\circ C)$	45	W
$R_{DS(ON)}(at V_{GS}=4.5V)$	<1.6	Ω

Application

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)
- Switch Mode Power Supply (SMPS)



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY5N50D	TO-252	MY5N50D	2500
MY5N50Y	TO-251	MY5N50Y	4000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Max.		Units
		TO-251/TO-252		
V_{DSS}	Drain-Source Voltage	500		V
V_{GSS}	Gate-Source Voltage	± 30		V
I_D	Continuous Drain Current	$T_C = 25^\circ C$	5	A
		$T_C = 100^\circ C$	3.4	A
I_{DM}	Pulsed Drain Current ^{note1}	20		A
E_{AS}	Single Pulsed Avalanche Energy ^{note2}	90		mJ
P_D	Power Dissipation	$T_C = 25^\circ C$	45	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.8		$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60		$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ C$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	500	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500V, V _{GS} = 0V, T _J = 25°C	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static Drain-Source On-Resistance ^{note3}	V _{GS} = 10V, I _D = 2.5A	-	1.35	1.6	Ω
C _{iss}	Input Capacitance	V _{DS} = 25V, V _{GS} = 0V, f = 1.0MHz	-	462	-	pF
C _{oss}	Output Capacitance		-	54.2	-	pF
C _{rss}	Reverse Transfer Capacitance		-	8.8	-	pF
Q _g	Total Gate Charge	V _{DD} = 400V, I _D = 5A, V _{GS} = 10V	-	13.5	-	nC
Q _{gs}	Gate-Source Charge		-	2	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	6	-	nC
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250V, I _D = 5A, R _G = 25Ω	-	10	-	ns
t _r	Turn-On Rise Time		-	25	-	ns
t _{d(off)}	Turn-Off Delay Time		-	40	-	ns
t _f	Turn-Off Fall Time		-	52	-	ns
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	20	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 5A, T _J = 25°C	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _S = 5A, di/dt = 100A/μs	-	220	-	ns
Q _{rr}	Reverse Recovery Charge		-	3	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 3A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

Typical Characteristics

Figure 1: Output Characteristics

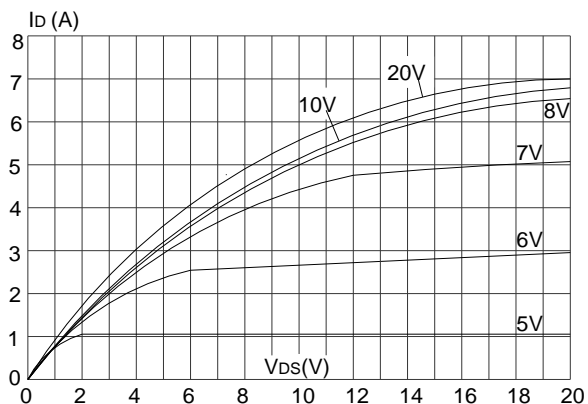


Figure 2: Typical Transfer Characteristics

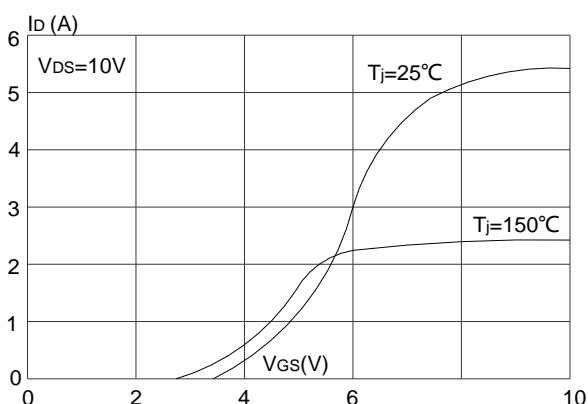


Figure 3: On-resistance vs. Drain Current

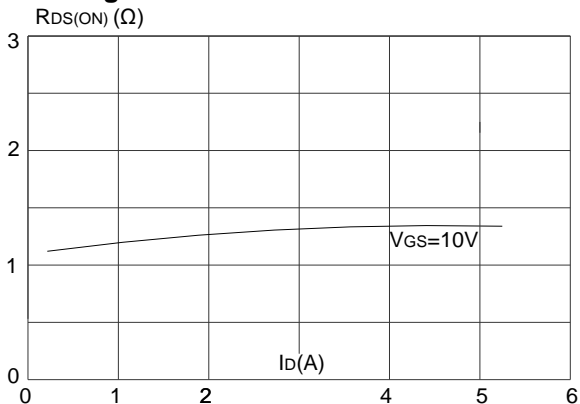


Figure 4: Body Diode Characteristics

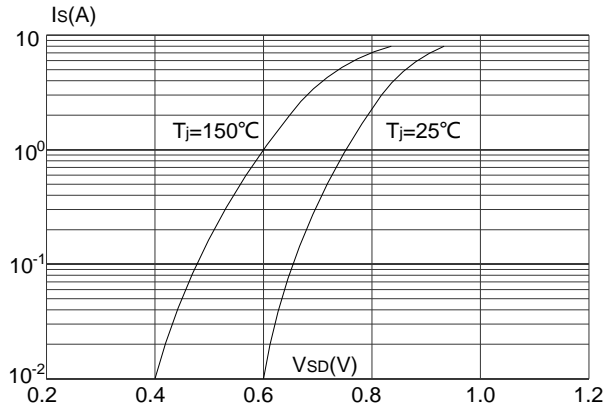


Figure 5: Gate Charge Characteristics

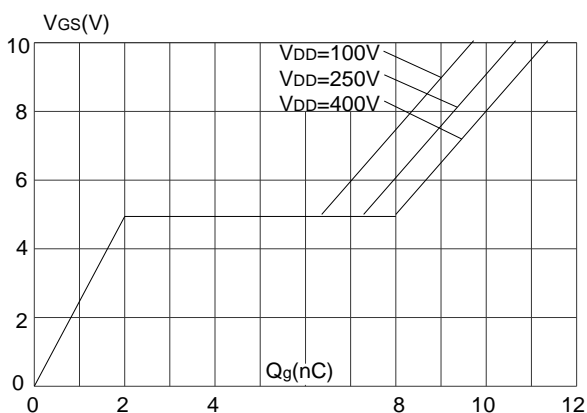


Figure 6: Capacitance Characteristics

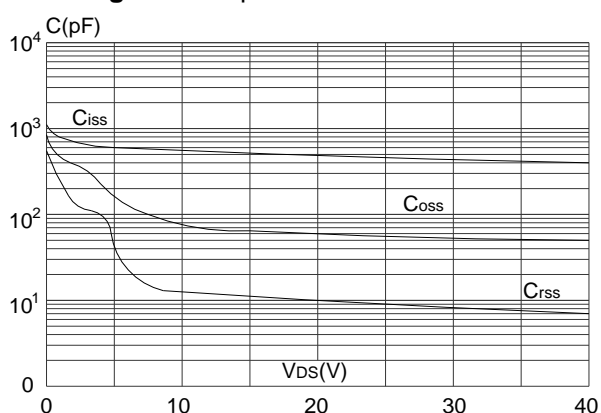


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

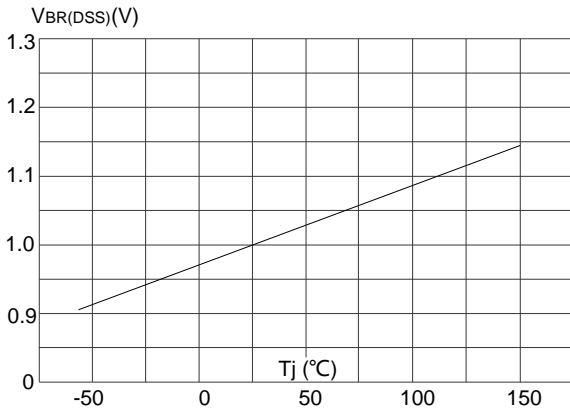


Figure 8: Normalized on Resistance vs. Junction Temperature

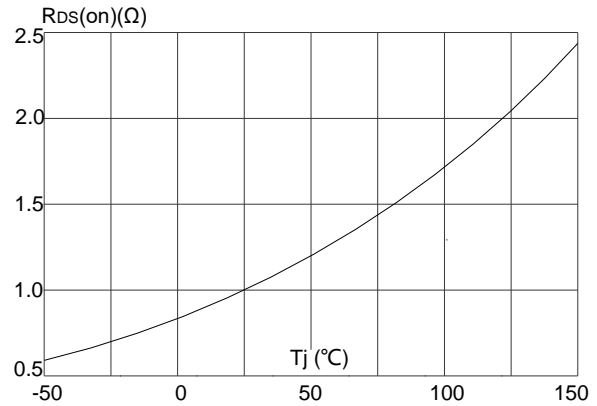


Figure 9: Maximum Safe Operating Area

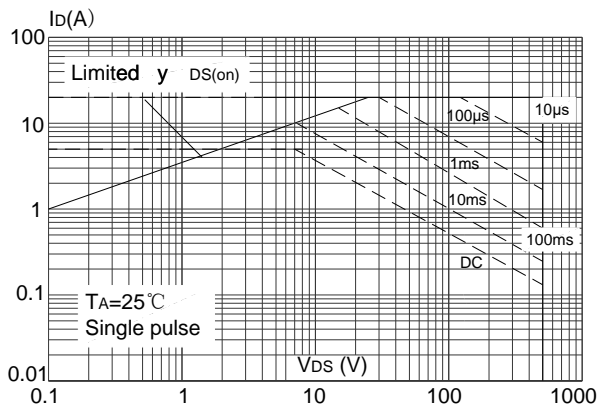


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

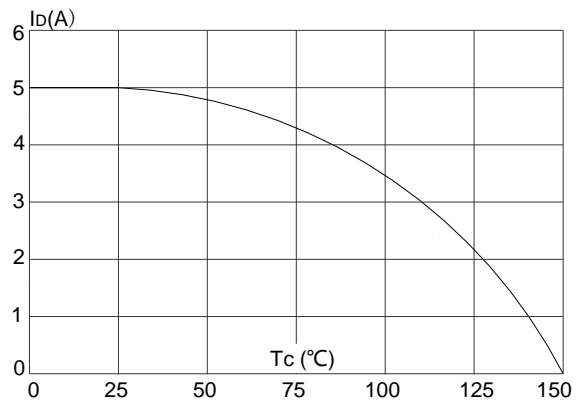


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220C, TO-251, TO-251S, TO-252)

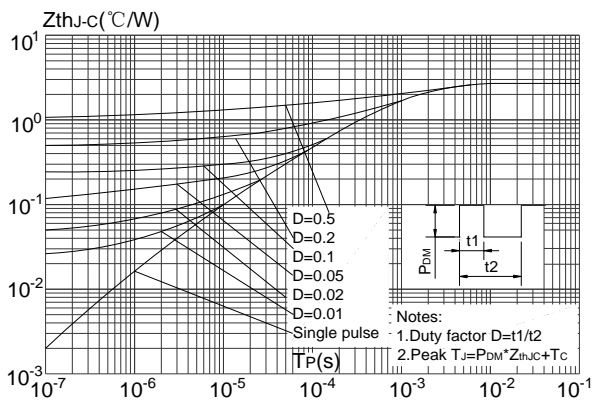
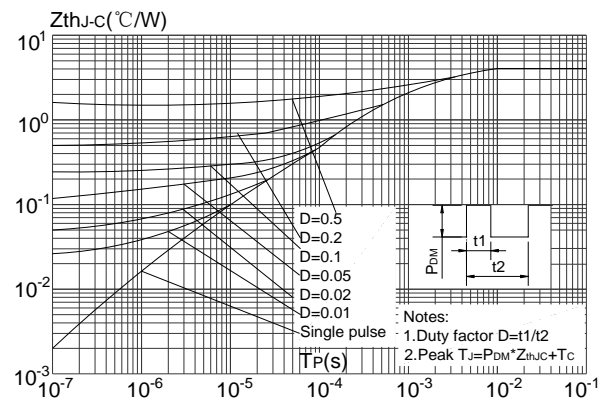


Figure.12: Maximum Effective Transient Thermal Impedance, Junction-to-Case (TO-220F)



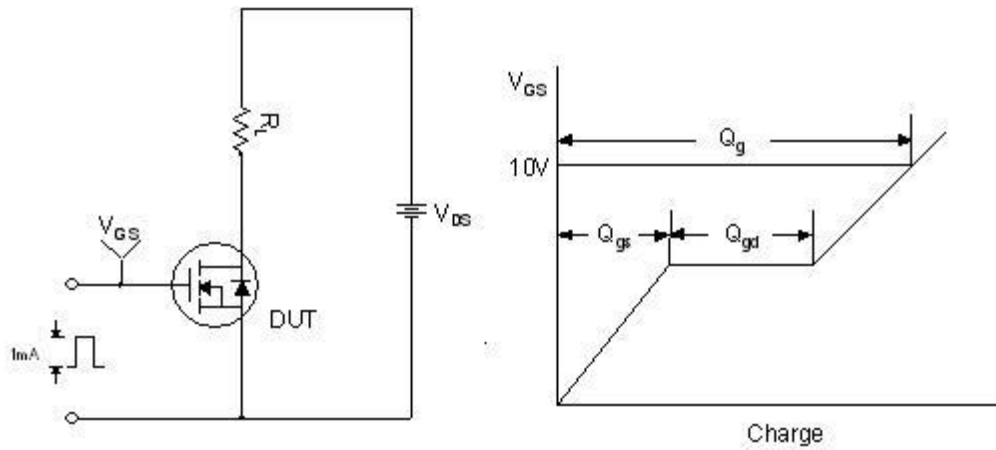


Figure 13. Gate Charge Test Circuit & Waveform

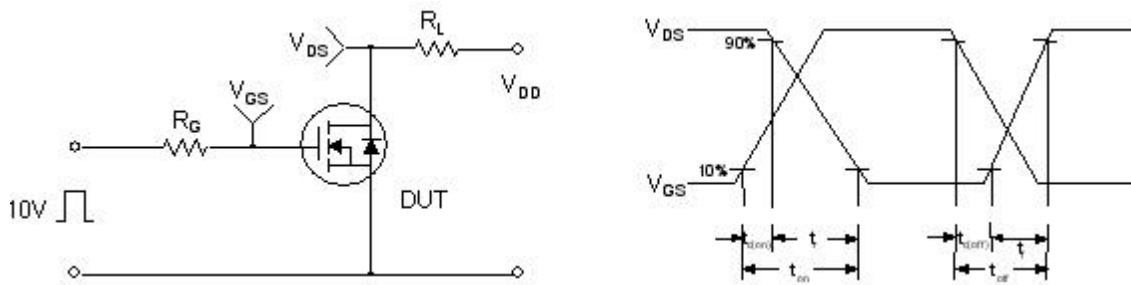


Figure 14. Resistive Switching Test Circuit & Waveforms

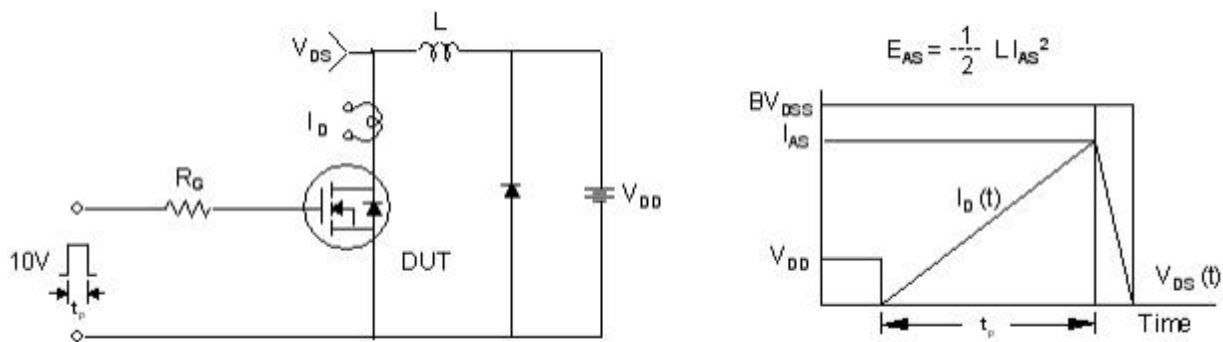
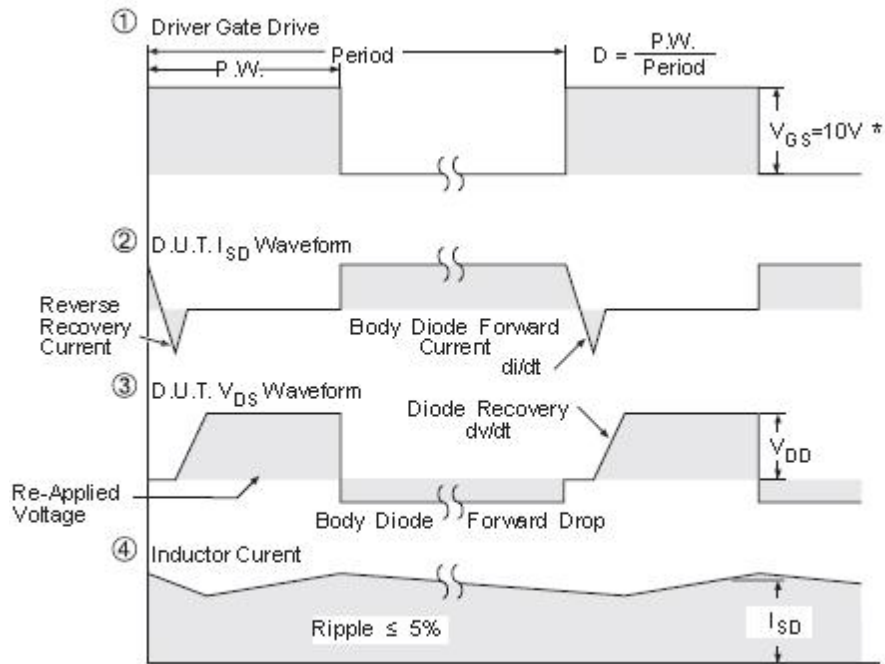
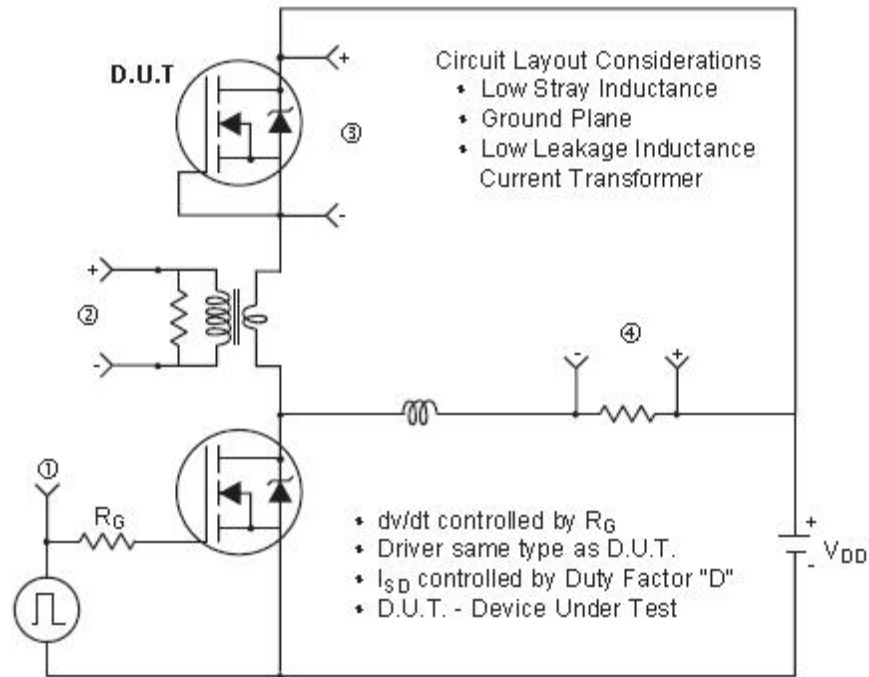


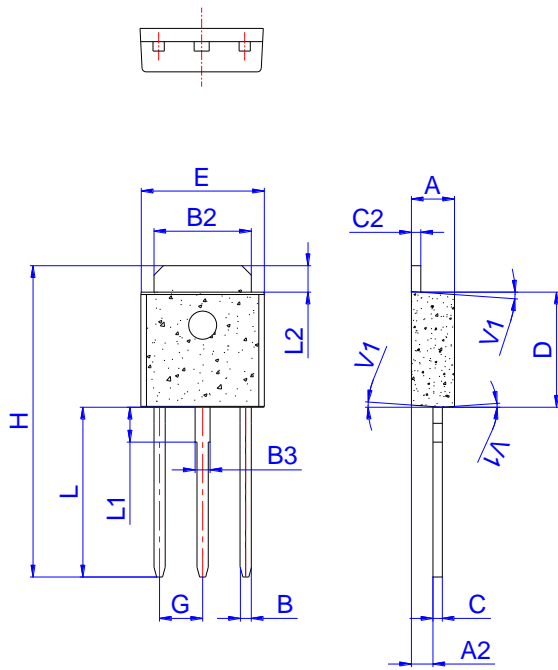
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



* $V_{GS} = 5V$ for Logic Level Devices

Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

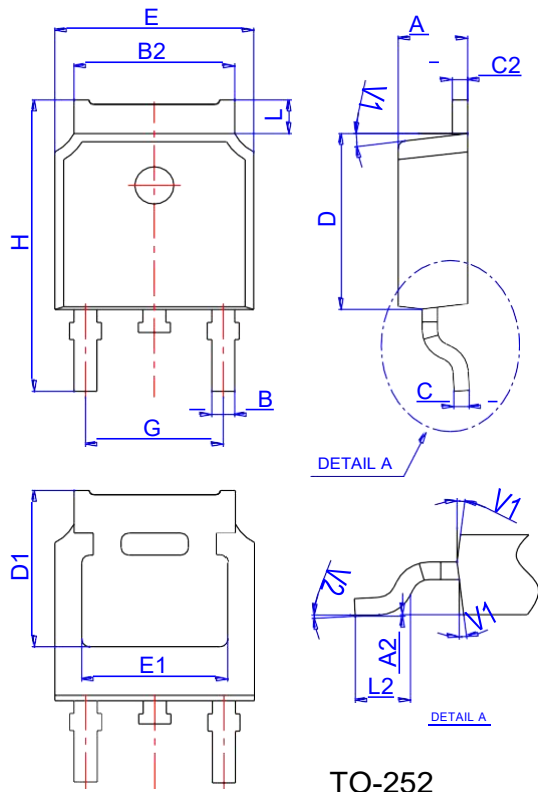
Package Mechanical Data



TO-251

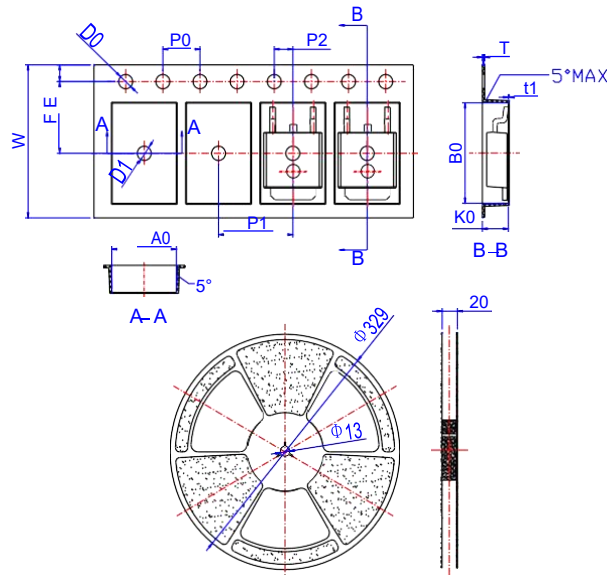
Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.086		0.095
A2	0.90		1.20	0.035		0.047
B	0.55		0.65	0.022		0.026
B2	5.10		5.40	0.200		0.213
B3	0.76		0.85	0.030		0.033
C	0.45		0.62	0.018		0.024
C2	0.48		0.62	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.70	0.252		0.264
G		2.30			0.091	
H	16.0		17.0	0.630		0.669
L	8.90		9.40	0.350		0.370
L1	1.80		1.90	0.071		0.075
L2	1.37		1.50	0.054		0.059
V1		4°			4°	

Package Mechanical Data-TO-252-JQ Single



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583