

## General Description

The MY18N20P is silicon N-channel Enhanced VDMOSFETs, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

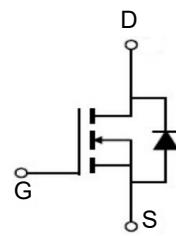
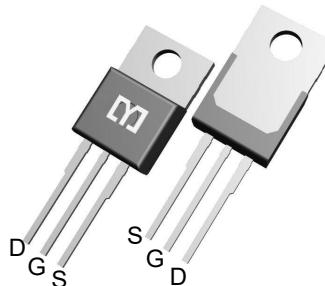


## Features

V <sub>DSS</sub>	200	V
I <sub>D</sub>	18	A
P <sub>D</sub> (T <sub>C</sub> =25°C)	125	W
R <sub>DS(ON)</sub> (at V <sub>GS</sub> = 10V)	< 0.2	Ω

## Application

- High efficiency switch mode power supplies
- Power factor correction
- Electronic lamp ballast



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY18N20P	TO-220	MY18N20P	1000

## Absolute Maximum Ratings (T<sub>c</sub>=25 °C unless otherwise noted)

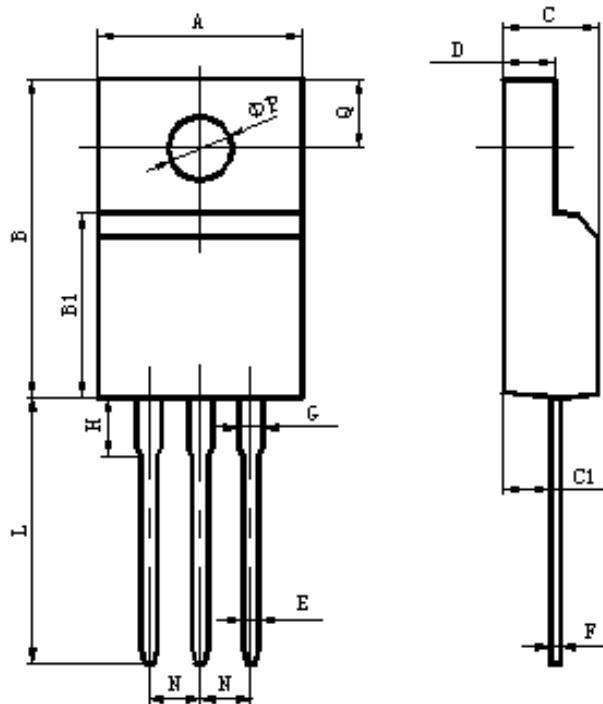
Symbol	Parameters	Ratings	Unit
V <sub>DSS</sub>	Drain-Source Voltage	200	V
V <sub>GS</sub>	Gate-Source Voltage-Continuous	±20	V
I <sub>D</sub>	Drain Current-Continuous (Note 2)	18	A
I <sub>DM</sub>	Drain Current-Single Plused (Note 1)	72	A
P <sub>D</sub>	Power Dissipation (Note 2)	125	W
T <sub>j</sub>	Max.Operating junction temperature	150	°C/W

Electrical Characteristics ( $T_c=25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameters	Min	Typ	Max	Units	Conditions
<b>Static Characteristics</b>						
$B_{VDSS}$	Drain-Source Breakdown VoltageCurrent (Note 1)	200	--	--	mA	$I_D=250\mu\text{A}$ $V_{GS}=0\text{V}$ , $T_J=25^\circ\text{C}$
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	--	4.0	V	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$
$R_{DS(\text{on})}$	Drain-Source On-Resistance	--	0.15	0.2	$\Omega$	$V_{GS}=10\text{V}$ , $I_D=9\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	--	--	$\pm 100$	nA	$V_{GS}=\pm 20\text{V}$ , $V_{DS}=0$
$I_{DSS}$	Zero Gate Voltage Drain Current	--	--	1	$\mu\text{A}$	$V_{DS}=200\text{V}$ , $V_{GS}=0$
<b>Switching Characteristics</b>						
$T_{d(\text{on})}$	Turn-On Delay Time	--	10	14	ns	$V_{DS}=160\text{V}$ , $I_D=18\text{A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{V}$ (Note 2)
$T_r$	Rise Time	--	15	20	ns	
$T_{d(\text{off})}$	Turn-Off Delay Time	--	12	17	ns	
$T_f$	Fall Time	--	12	17	ns	
$Q_g$	Total Gate Charge	--	31	--	nC	$V_{DS}=160\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=18\text{A}$ (Note 2)
$Q_{gs}$	Gate-Source Charge	--	7.5	--	nC	
$Q_{gd}$	Gate-Drain Charge	--	9	--	nC	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	--	540	700	pF	$V_{DS}=25\text{V}$ , $V_{GS}=0$ , $f=1\text{MHz}$
$C_{oss}$	Output Capacitance	--	90	120	pF	
$C_{rss}$	Reverse Transfer Capacitance	--	35	50	pF	
$I_s$	Continuous Drain-Source Diode Forward Current (Note 2)	--	--	18	A	
$V_{SD}$	Diode Forward On-Voltage	--	--	1.4	V	$I_s=9\text{A}$ , $V_{GS}=0$
$R_{th(j-c)}$	Thermal Resistance, Junction to Case	--	--	2.0	C/ W	

Note 1: Repetitive Rating : Pulse width limited by maximum junction temperature

Note 2: Pulse test: PW &lt;= 300us , duty cycle &lt;= 2%.

**Package Mechanical Data-TO-220 Single**


Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.40	2.90
L*	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
P	2.90	3.30