

## General Description

The MY180N10NE5 uses advanced trench technology to provide excellent  $R_{DS(on)}$ , low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

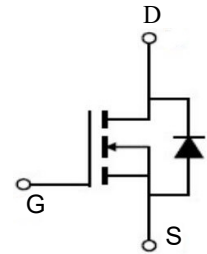
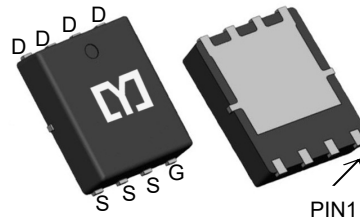


## Features

$X_{FUU}$	100	X
$K$	180	C
$P_D(T_C=25^\circ C)$	152	W
$T_{FUTQP} \#cXI U? 10X+$	> 4.5	o á

## Application

- Low  $R_{DS(on)}$  & FOM
- Extremely low switching loss
- Excellent stability and uniformity or Invertors



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY180N10NE5	PDFN5*6-8L	NULL	5000

## Absolute Maximum Ratings ( $T_J=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain source voltage	$V_{DS}$	100	V
Gate source voltage	$V_{GS}$	$\pm 20$	V
Continuous drain current <sup>1)</sup> , $T_C=25^\circ C$	$I_D$	180	A
Pulsed drain current <sup>2)</sup> , $T_C=25^\circ C$	$I_D, \text{ pulse}$	360	A
Power dissipation <sup>3)</sup> $T_C=25^\circ C$	$P_D$	152	W
Single pulsed avalanche energy <sup>5)</sup>	$E_{AS}$	400	mJ
Operation and storage temperature	$T_{stg}, T_j$	-55 to 175	$^\circ C$
Thermal resistance, junction-case	$R_{\theta JC}$	0.65	$^\circ C/W$
Thermal resistance, junction-ambient <sup>4)</sup>	$R_{\theta JA}$	62	$^\circ C/W$

**Electrical Characteristics ( $T_J=25\text{ }^\circ\text{C}$ , unless otherwise noted)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	$BV_{DSS}$	100			V	$V_{GS}=0\text{ V}$ , $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	2.0		4.0	V	$V_{DS}=V_{GS}$ , $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(on)}$		3.6	4.5	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$
Gate-source leakage current	$I_{GSS}$			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	$I_{DSS}$			1	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$
Input capacitance	$C_{iss}$		6920		pF	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$		1026		pF	
Reverse transfer capacitance	$C_{rss}$		33		pF	
Turn-on delay time	$t_{d(on)}$		48		ns	$V_{GS}=10\text{ V}$ , $V_{DS}=50\text{ V}$ , $R_G=2.2\text{ }\Omega$ , $I_D=22\text{ A}$
Rise time	$t_r$		56		ns	
Turn-off delay time	$t_{d(off)}$		75		ns	
Fall time	$t_f$		33		ns	
Total gate charge	$Q_g$		117		nC	$I_D=22\text{ A}$ , $V_{DS}=50\text{ V}$ , $V_{GS}=10\text{ V}$
Gate-source charge	$Q_{gs}$		40		nC	
Gate-drain charge	$Q_{gd}$		37		nC	
Gate plateau voltage	$V_{plateau}$		4.2		V	
Diode forward current	$I_S$			130	A	$V_{GS}<V_{th}$
Pulsed source current	$I_{SP}$			390		
Diode forward voltage	$V_{SD}$			1.3	V	$I_S=20\text{ A}$ , $V_{GS}=0\text{ V}$
Reverse recovery time	$t_{rr}$		82.1		ns	$I_S=10\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$		248.4		nC	
Peak reverse recovery current	$I_{rrm}$		4.9		A	

**Note**

- 1、Calculated continuous current based on maximum allowable junction temperature.
- 2、Repetitive rating; pulse width limited by max. junction temperature.
- 3、Pd is based on max. junction temperature, using junction-case thermal resistance.
- 4、The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_a=25\text{ }^\circ\text{C}$ .
- 5、 $V_{DD}=50\text{ V}$ ,  $R_G=25\text{ }\Omega$ ,  $L=0.5\text{ mH}$ , starting  $T_J=25\text{ }^\circ\text{C}$ .

**Typical Characteristics**

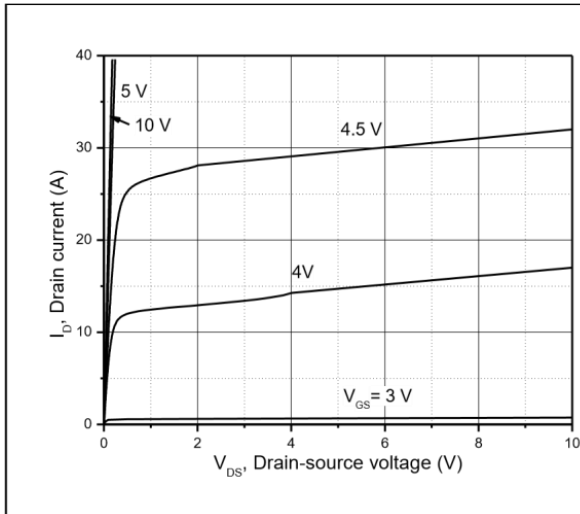


Figure 1, Typ. output characteristics

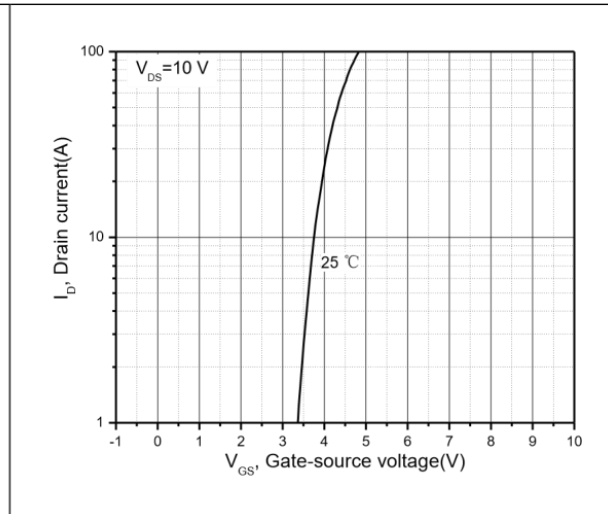


Figure 2, Typ. transfer characteristics

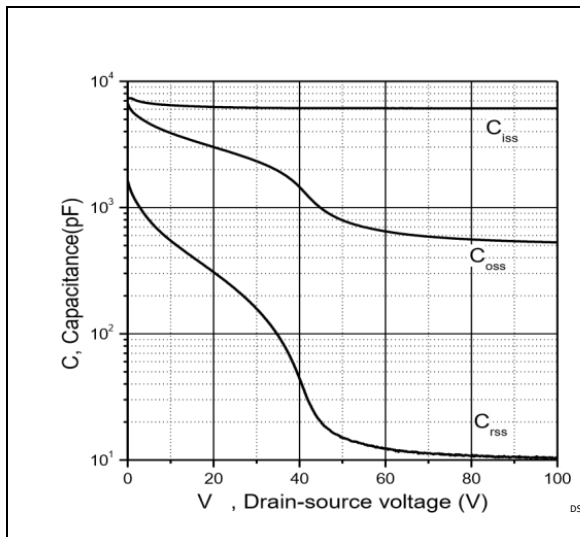


Figure 3, Typ. capacitances

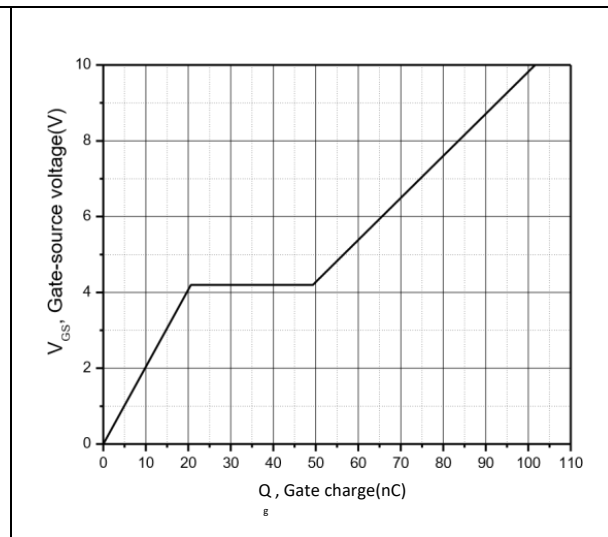


Figure 4, Typ. gate charge

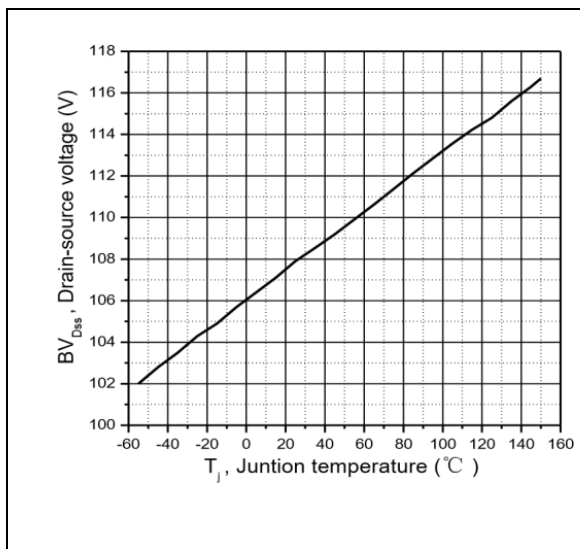


Figure 5, Drain-source breakdown voltage

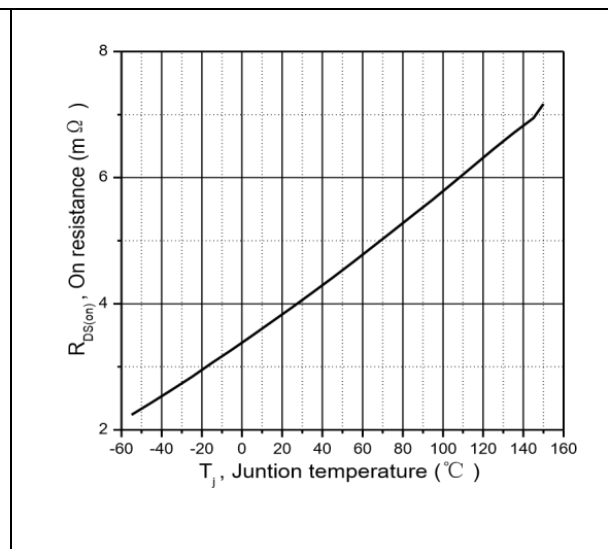


Figure 6, Drain-source on-state resistance

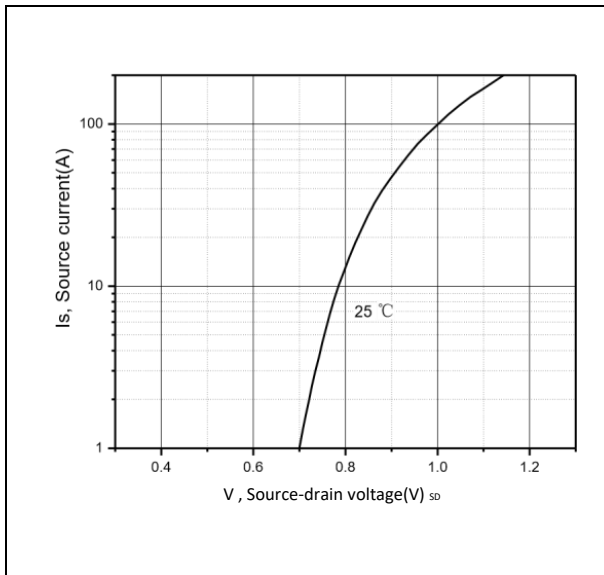


Figure 7, Forward characteristic of body diode

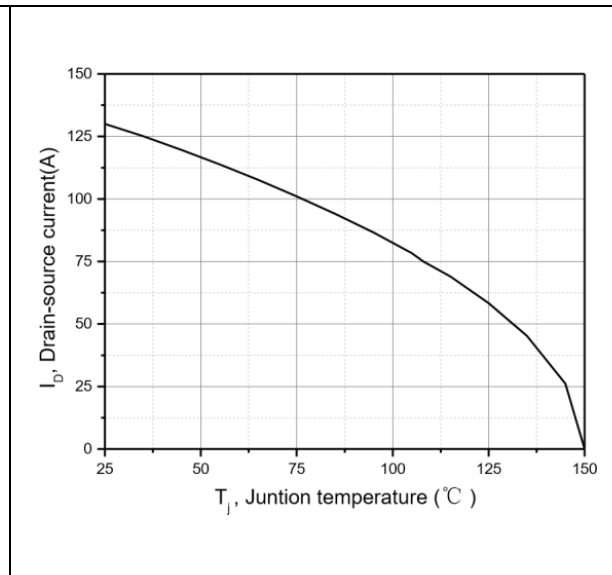


Figure 8, Drain current

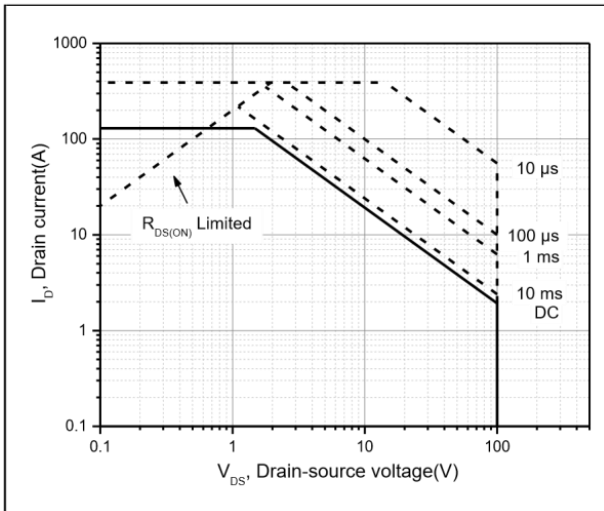


Figure 9, Safe operation area for TO220/TO263  
 $T_C=25\text{ °C}$

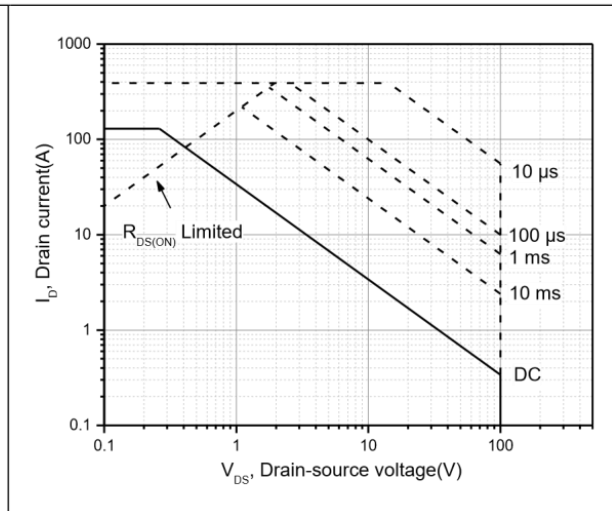


Figure 10, Safe operation area for TO220F  
 $T_C=25\text{ °C}$

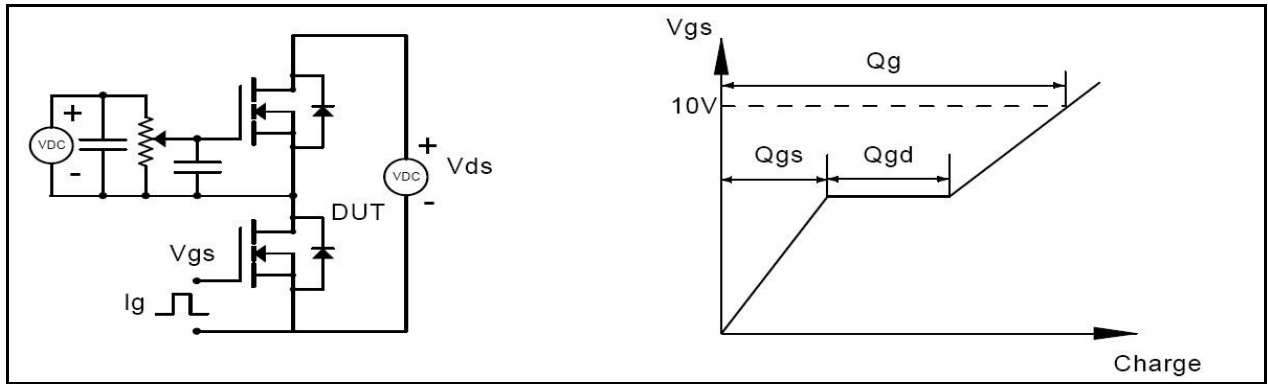


Figure 1, Gate charge test circuit & waveform

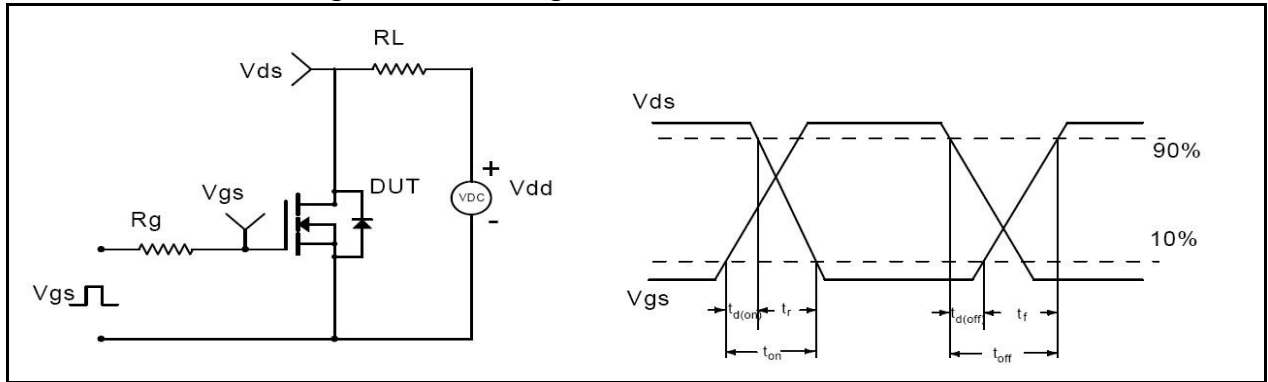


Figure 2, Switching time test circuit & waveforms

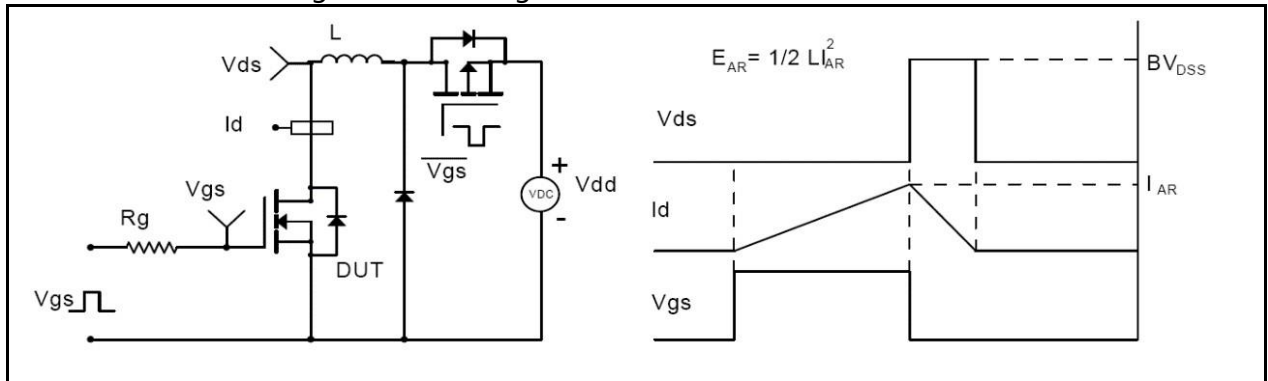


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

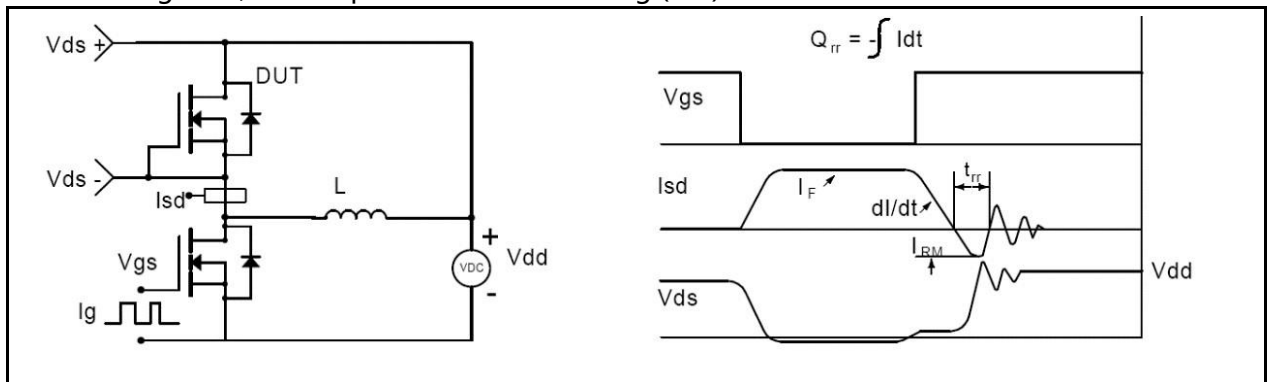
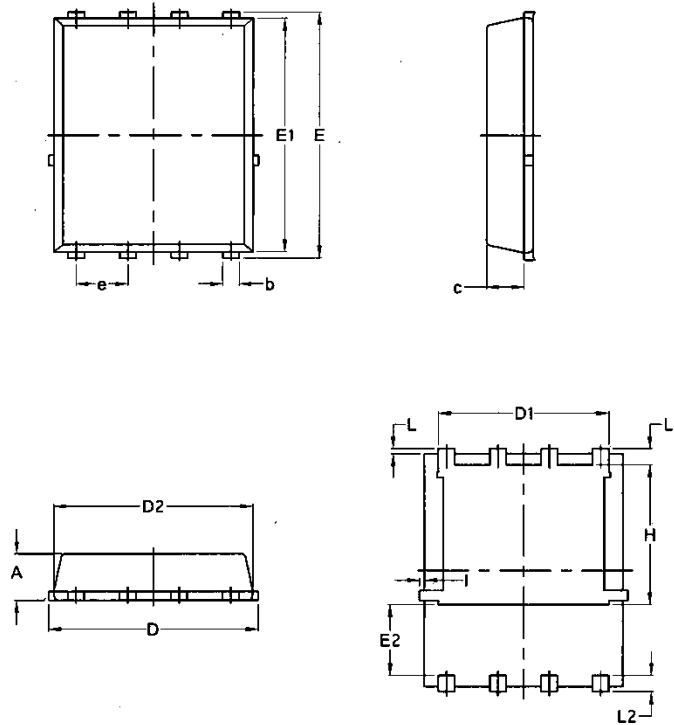


Figure 4, Diode reverse recovery test circuit & waveforms

**Package Mechanical Data-DFN5\*6-8L-JQ Single**



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070