MY150N03NE3

30V N-Channel Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

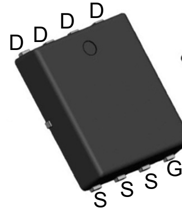
The MY150N03NE3 uses Fast switching MOSFET for SMPS Very low on-resistance RDS(on) and Optimized technology for DC/DC converters.

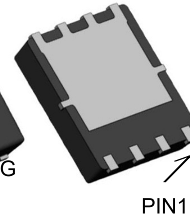
Features

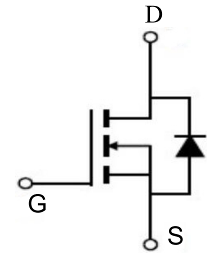
V_{DSS}	30	V
I_D	150	A
$R_{DS(ON)(atV_{GS}=10V)}$	1.3	mΩ
$R_{DS(ON)(atV_{GS}=4.5V)}$	1.8	mΩ

Application

- logic level
- Superior thermal resistance
- 100 valanche tested
- P-free plating







Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY150N03NE3	PDFN3*3-8L	NULL	5000

Absolute Maximum Ratings (T_J=25℃unless otherwise noted)

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, T_C=25 °C	150	A
		V_{GS}=10 V, T_C=100 °C	120	
		V_{GS}=4.5 V, T_C=25 °C	100	
		V_{GS}=4.5 V, T_C=100 °C	100	
		V_{GS}=10 V, T_A=25 °C, R_{thJA}=50 K/W[2)]	31	
Pulsed drain current[3)]	$I_{D,pulse}$	T_C=25 °C	400	
Avalanche current, single pulse[4)]	I_{AS}	T_C=25 °C	50	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	295	mJ
Gate source voltage	V_{GS}		±20	V

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Parameter	Symbol	Conditions	Value	Unit
Power dissipation	P_{tot}	T_C=25 °C	139	W
		T_A=25 °C, R_{thJA}=50 K/W[2)]	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}	bottom	-	-	0.9	K/W
		top			20	
Device on PCB	R_{thJA}	6 cm² cooling area[2)]	-	-	50	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=85 µA	1.2	-	2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=50 A	-	1.8	2.3	mΩ
		V_{GS}=10 V, I_D=50 A	-	1.3	1.6	
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=50 A	95	190	-	S

[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3)] See figure 3 for more detailed information

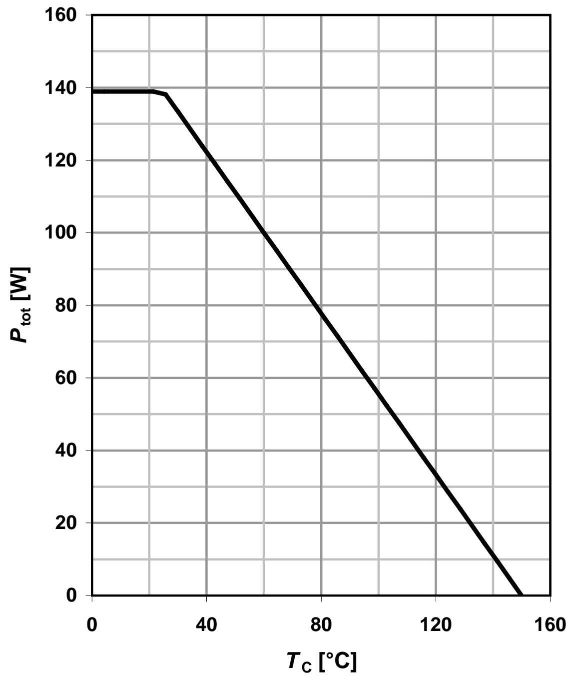
[4)] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=20 V, f =1 MHz	-	8900	12000	pF
Output capacitance	C_{oss}		-	1800	2400	
Reverse transfer capacitance	C_{rss}		-	100	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20 V, V_{GS}=10 V, I_D=30 A, R_G=1.6 Ω	-	14	-	ns
Rise time	t_r		-	7.6	-	
Turn-off delay time	$t_{d(off)}$		-	56	-	
Fall time	t_f		-	9.4	-	
Gate Charge Characteristics[5]						
Gate to source charge	Q_{gs}	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 10 V	-	25	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	14	-	
Gate to drain charge	Q_{gd}		-	11	-	
Switching charge	Q_{sw}		-	23	-	
Gate charge total	Q_g		-	113	150	
Gate plateau voltage	$V_{plateau}$		-	2.9	-	V
Gate charge total	Q_g	V_{DD}=20 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	54	-	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	V_{DS}=0.1 V, V_{GS} =0 to 10 V	-	106	-	
Output charge	Q_{oss}	V_{DD}=20 V, V_{GS}=0 V	-	69	-	
Reverse Diode						
Diode continuous forward current	I_S	T_C=25 °C	-	-	100	A
Diode pulse current	$I_{S,pulse}$		-	-	400	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=50 A, T_j=25 °C	-	0.8	1.2	V
Reverse recovery charge	Q_{rr}	V_R=20 V, I_F=I_S, di_F/dt=400 A/μs	-	125	-	nC

[5] See figure 16 for gate charge parameter definition

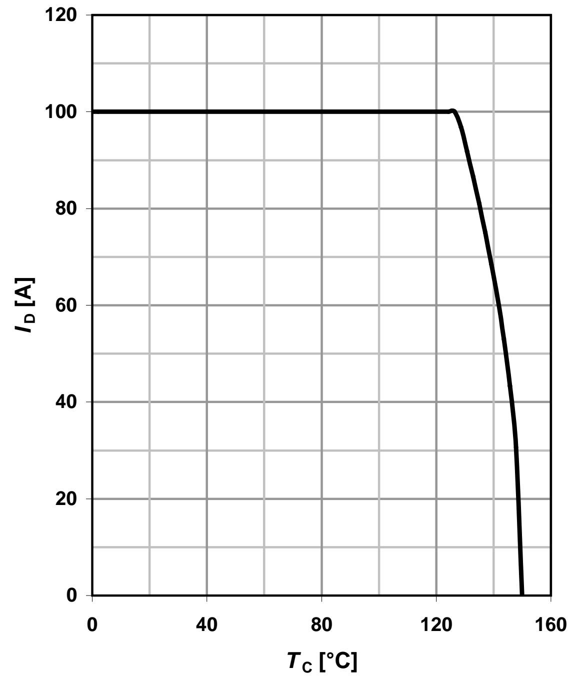
1 Power dissipation

P_{tot}=f(T_C)



2 Drain current

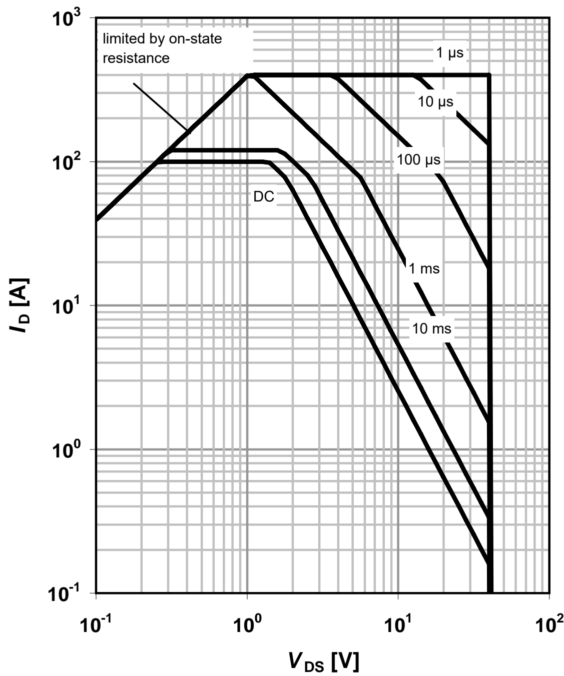
I_D=f(T_C); V_{GS}≥10 V



3 Safe operating area

I_D=f(V_{DS}); T_C=25 °C; D=0

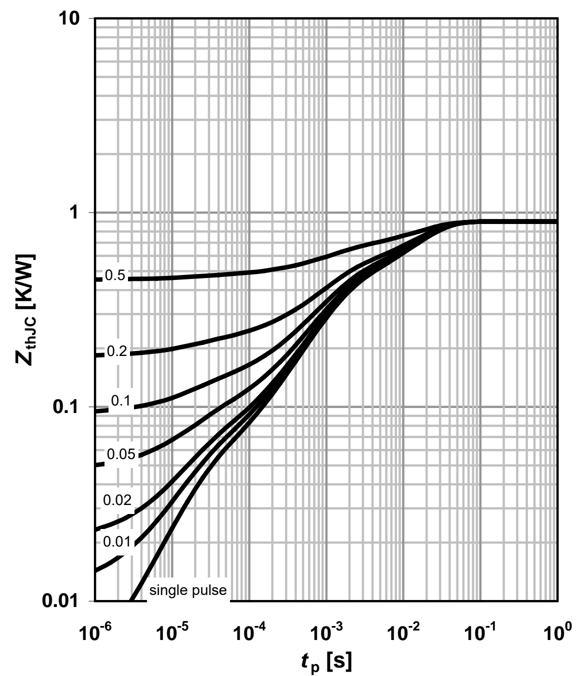
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC}=f(t_p)

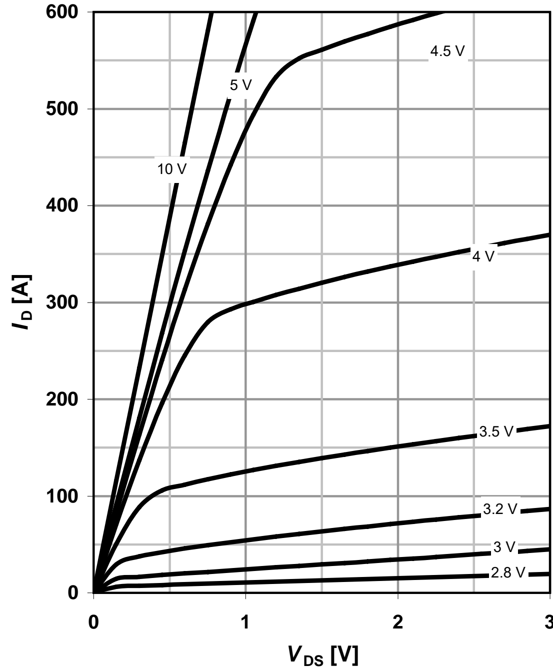
parameter: D=t_p/T



5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

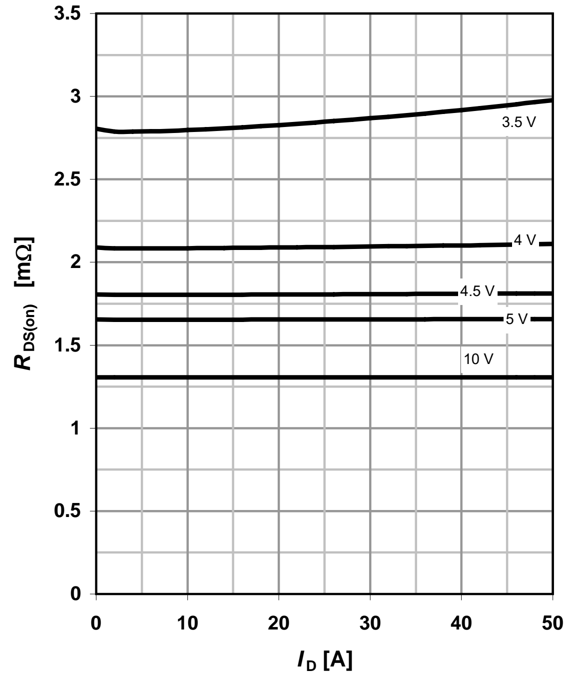
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

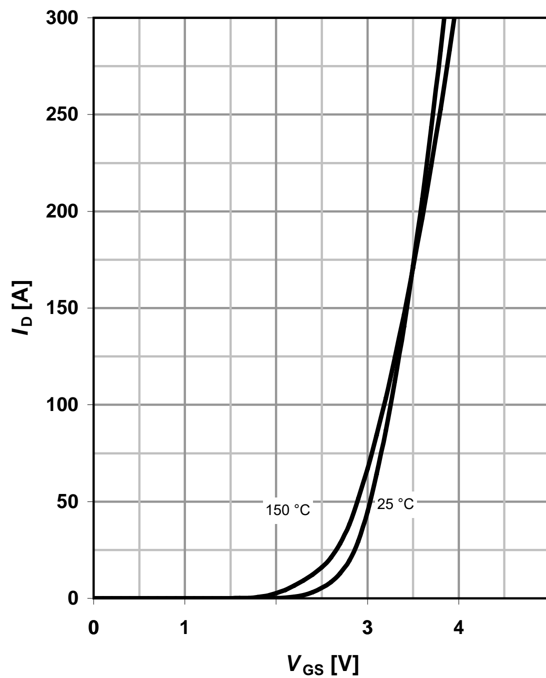
parameter: V_{GS}



7 Typ. transfer characteristics

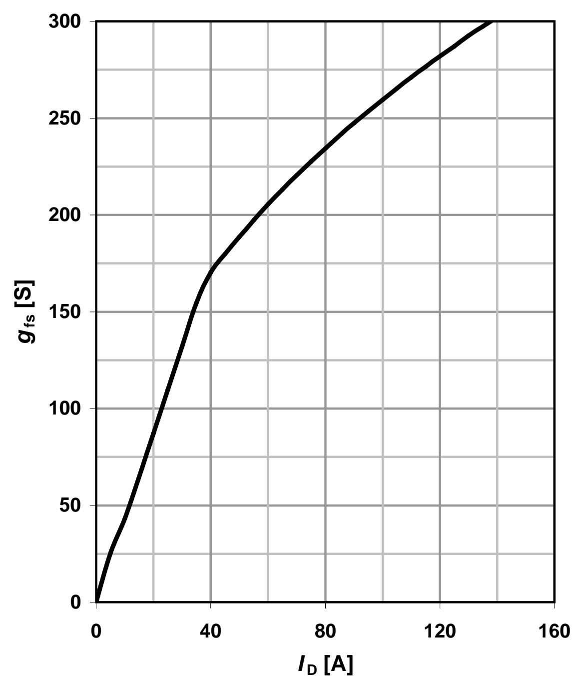
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



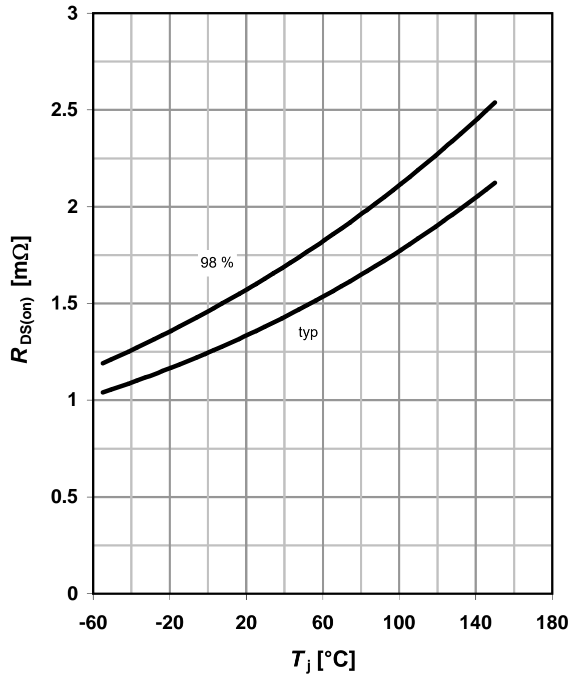
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



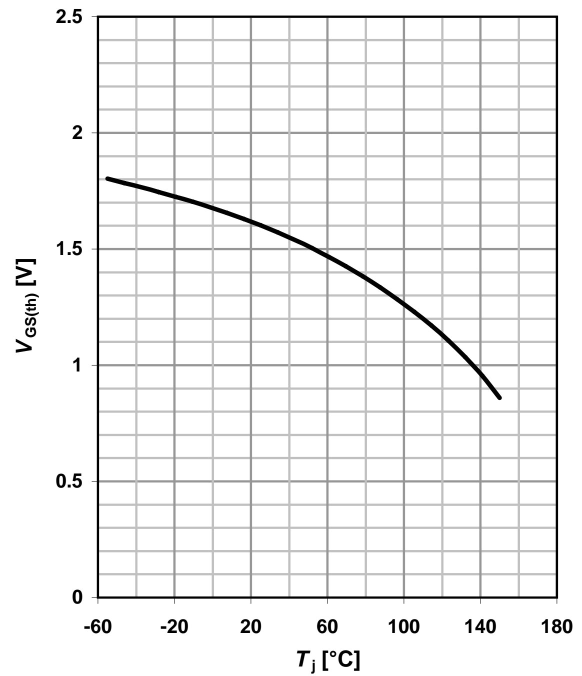
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=50 A; V_{GS}=10 V



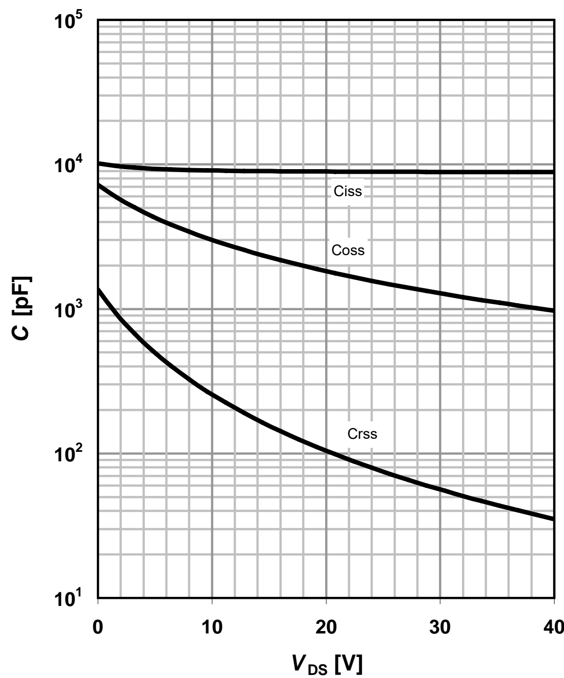
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=85 µA



11 Typ. capacitances

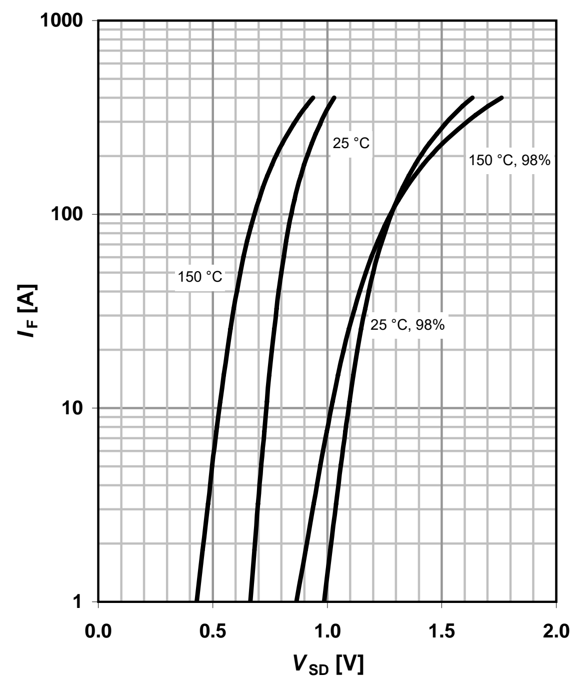
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

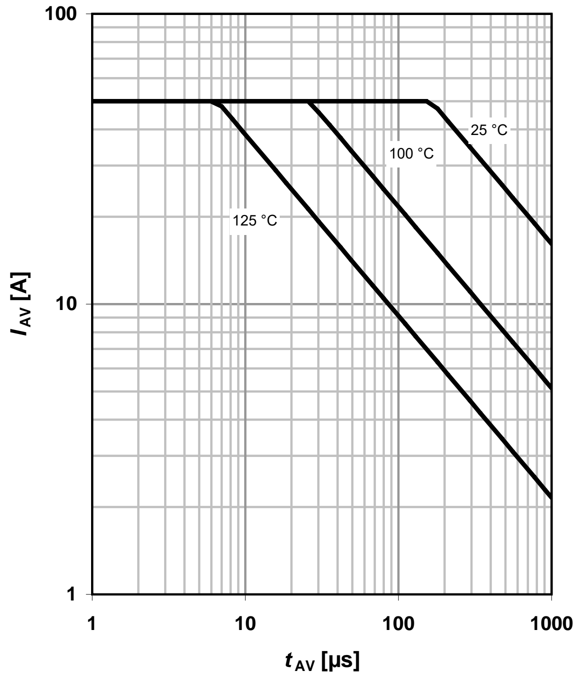
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

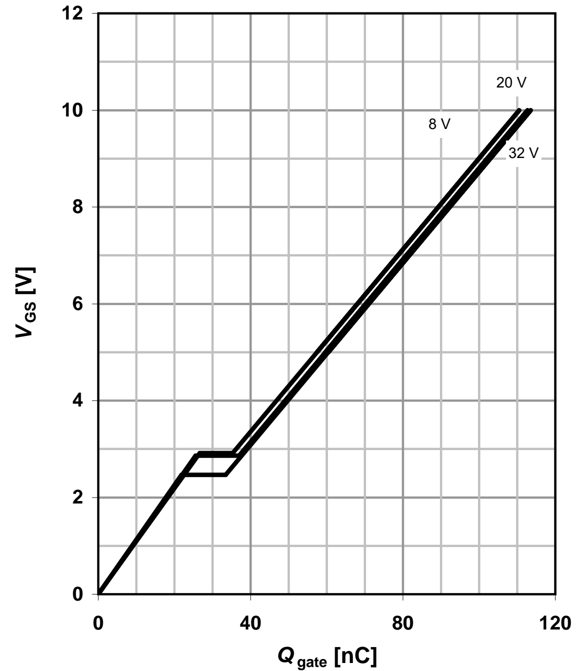
parameter: $T_{j(start)}$



14 Typ. gate charge

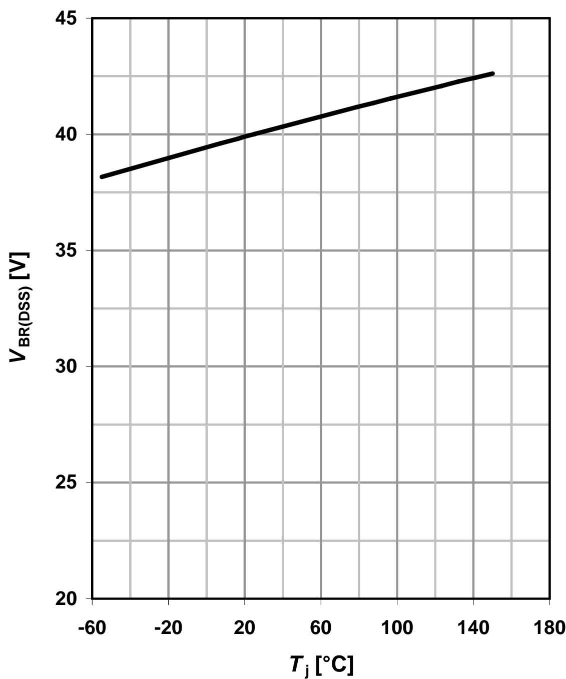
V_{GS}=f(Q_{gate}); I_D=30 A pulsed

parameter: V_{DD}

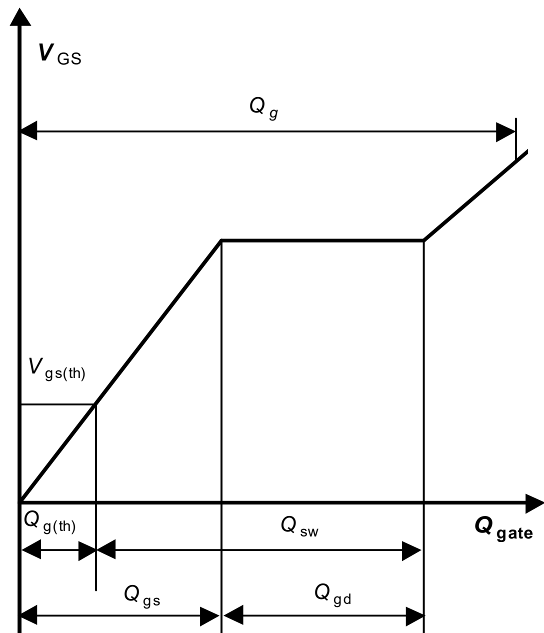


15 Drain-source breakdown voltage

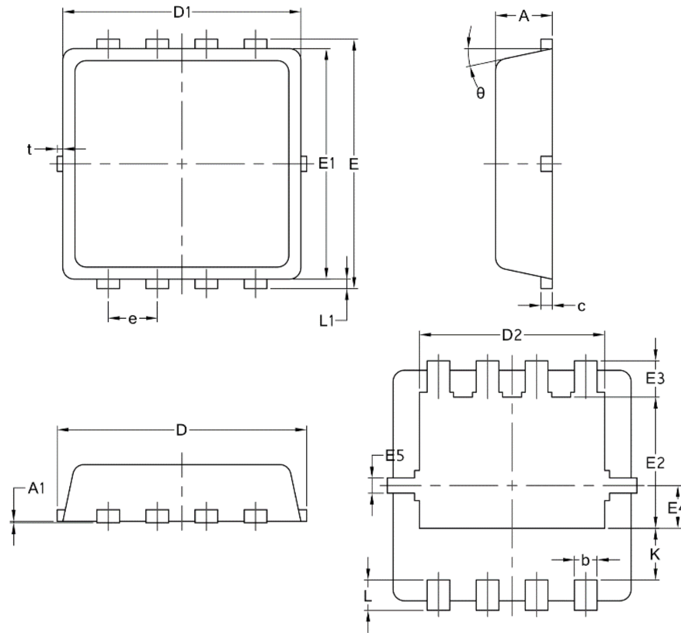
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Common		
	mm		
	Mim	Nom	Max
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
Φ	10	12	14