

### General Description

The MY100N10P is the high cell density trench N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The MY100N10P meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

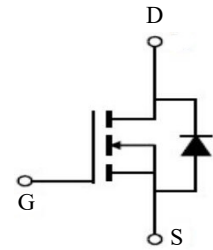
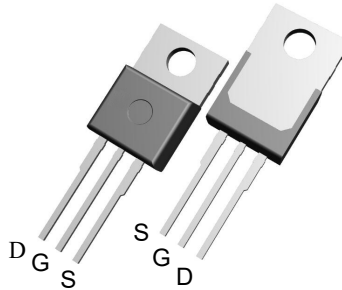


### Features

$V_{DSS}$	100	V
$I_D$	120	A
$R_{DS(ON)}(at V_{GS}=10V)$	4.6	m $\Omega$
$R_{DS(ON)}(at V_{GS}=8V)$	4.9	m $\Omega$

### Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY100N10P	TO-220	100N10P	1000

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup>	$I_D$	$T_C=25^\circ C$	120
		$T_C=100^\circ C$	73.4
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	464	A
Single Pulse Avalanche Energy <sup>3</sup>	<b>EAS</b>	205	mJ
Total Power Dissipation <sup>4</sup>	$P_D$	162	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	$^\circ C$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>1</sup>	$R_{\theta JA}$	58	$^\circ C/W$
Thermal Resistance from Junction-to-Case <sup>1</sup>	$R_{\theta JC}$	0.77	$^\circ C/W$



### Electrical Characteristics at $T_J=25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
Gate-body Leakage current	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$T_J=25^\circ\text{C}$	$I_{DSS}$ $V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
	$T_J=100^\circ\text{C}$		-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.2	2.9	3.6	V
Drain-Source on-Resistance <sup>2</sup>	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	4.6	6	m $\Omega$
		$V_{GS} = 8.0V, I_D = 15A$	-	4.9	6.5	
<b>Dynamic Characteristics</b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 50V, V_{GS} = 0V,$ $f = 1MHz$	-	4400	-	pF
Output Capacitance	$C_{oss}$		-	645	-	
Reverse Transfer Capacitance	$C_{rss}$		-	20	-	
<b>Switching Characteristics</b>						
Gate Resistance	$R_g$	$V_{GS} = 0V, V_{DS} = 0V,$ $f = 1MHz$	-	1.6	-	$\Omega$
Total Gate Charge	$Q_g$	$V_{GS} = 10V, V_{DS} = 50V,$ $I_D = 20A$	-	75	-	nC
Gate-Source Charge	$Q_{gs}$		-	17	-	
Gate-Drain Charge	$Q_{gd}$		-	13	-	
Turn-on Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DS} = 50V,$ $R_G = 3\Omega, I_D = 20A$	-	15.4	-	ns
Rise Time	$t_r$		-	13	-	
Turn-off Delay Time	$t_{d(off)}$		-	34	-	
Fall Time	$t_f$		-	6.2	-	
<b>Drain-Source Body Diode Characteristics</b>						
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	$I_F = 20A, V_{GS} = 0V$	-	-	1.2	V
Continuous Source Current <sup>1,5</sup>	$I_S$	$V_G=V_D=0V$ , Force Current	-	-	120	A
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 20A, di/dt=100A/\mu s$	-	55	-	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		-	101	-	nC

Notes:

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- The EAS data shows Max. rating. The test condition is  $V_{DD}=50V, V_{GS}=10V, L=0.4mH, I_{AS}=32A$
- The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.



**Typical Characteristics**

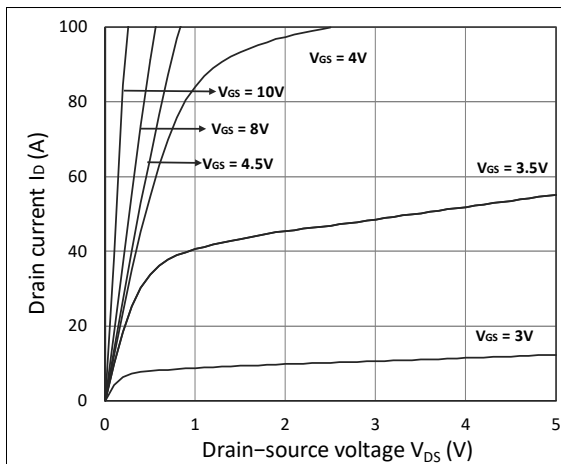


Figure 1. Output Characteristics

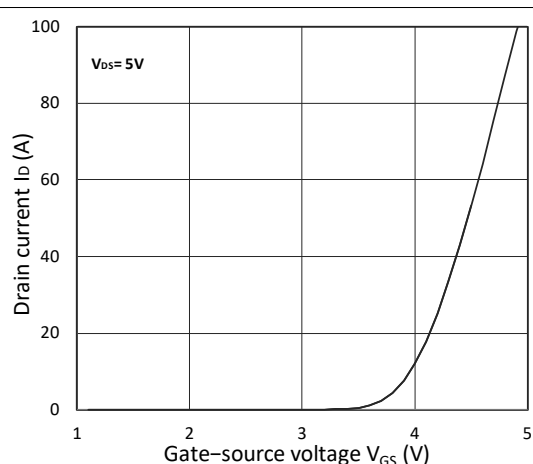


Figure 2. Transfer Characteristics

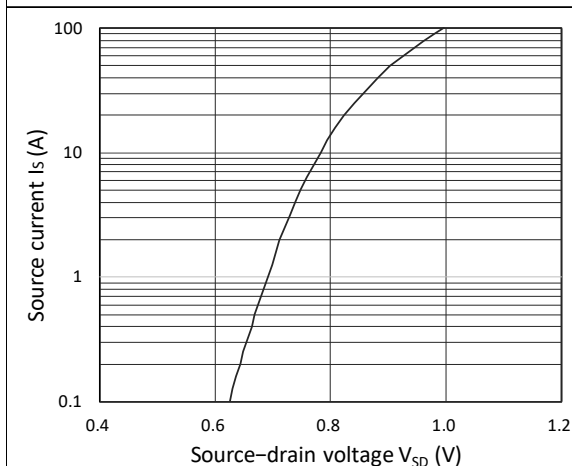


Figure 3. Forward Characteristics of Reverse

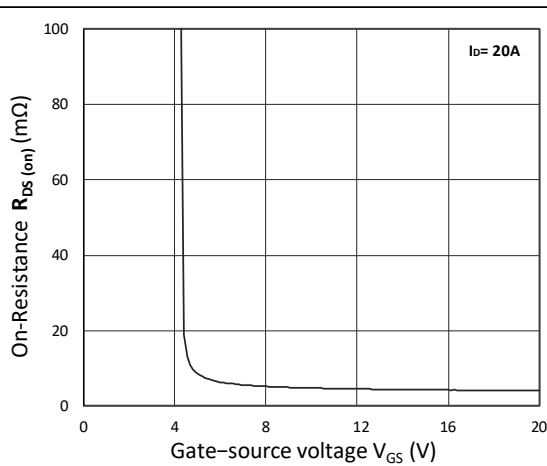


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

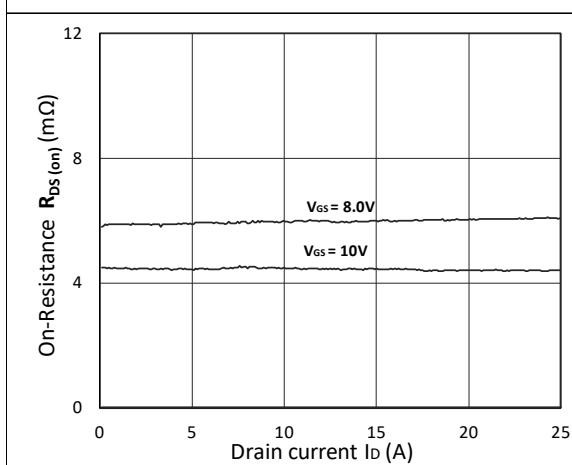


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

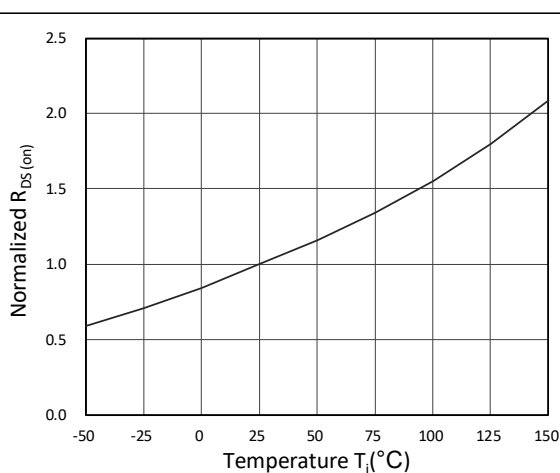


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

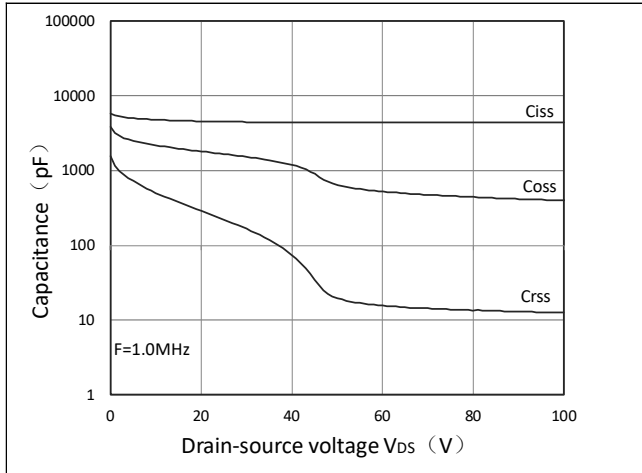


Figure 7. Capacitance Characteristics

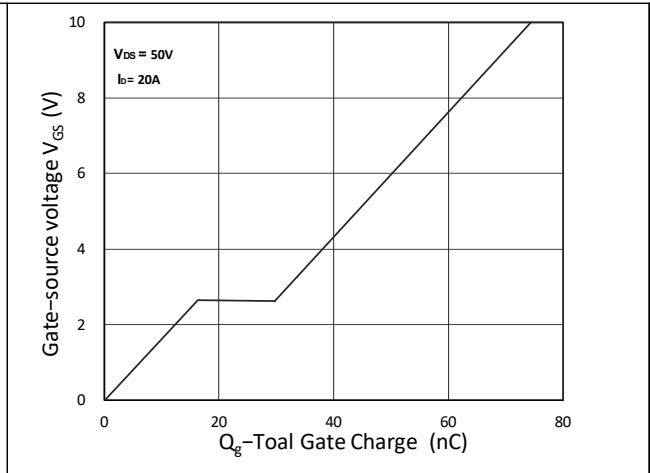


Figure 8. Gate Charge Characteristics

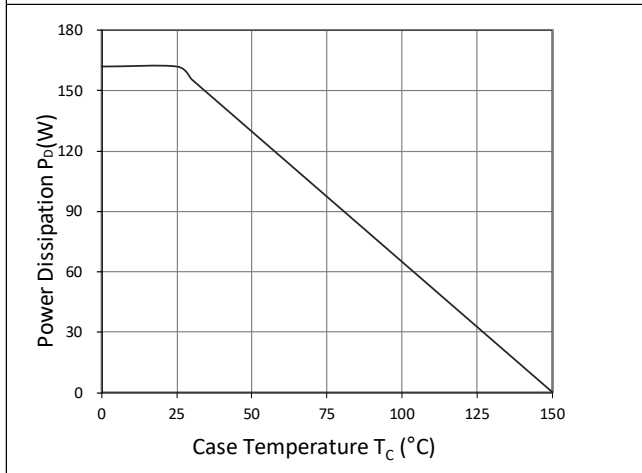


Figure 9. Power Dissipation

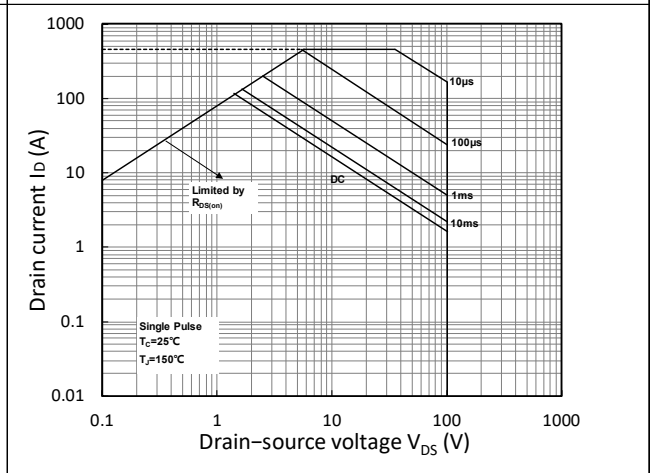


Figure 10. Safe Operating Area

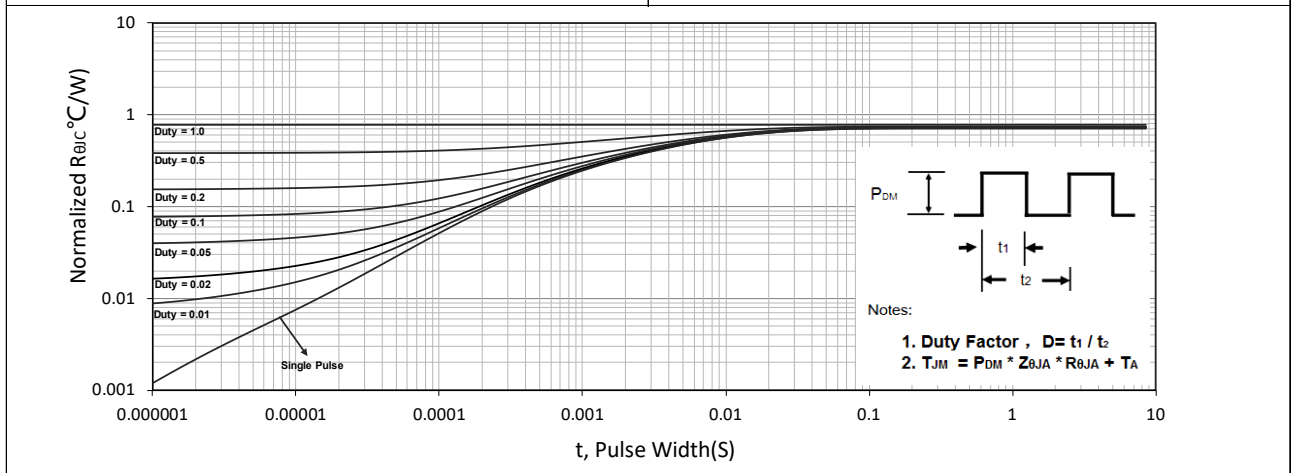
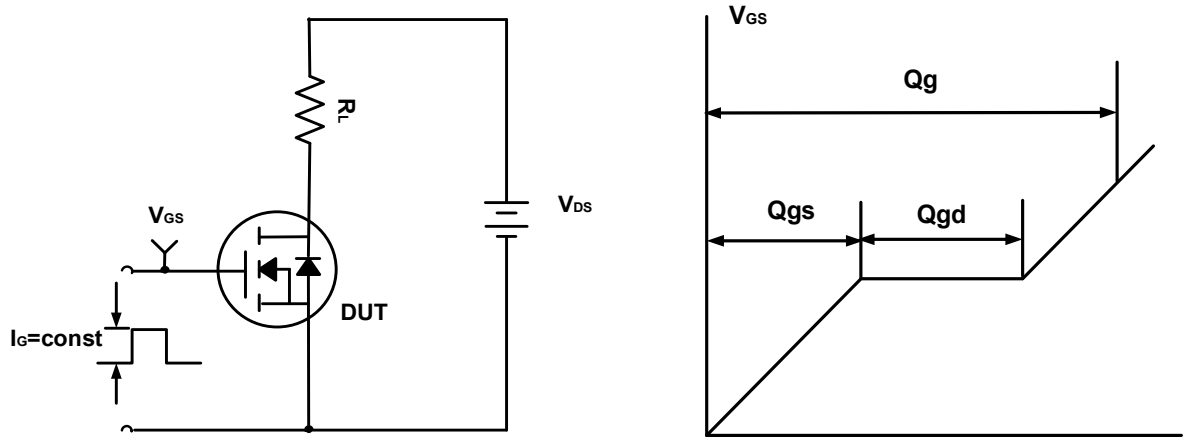
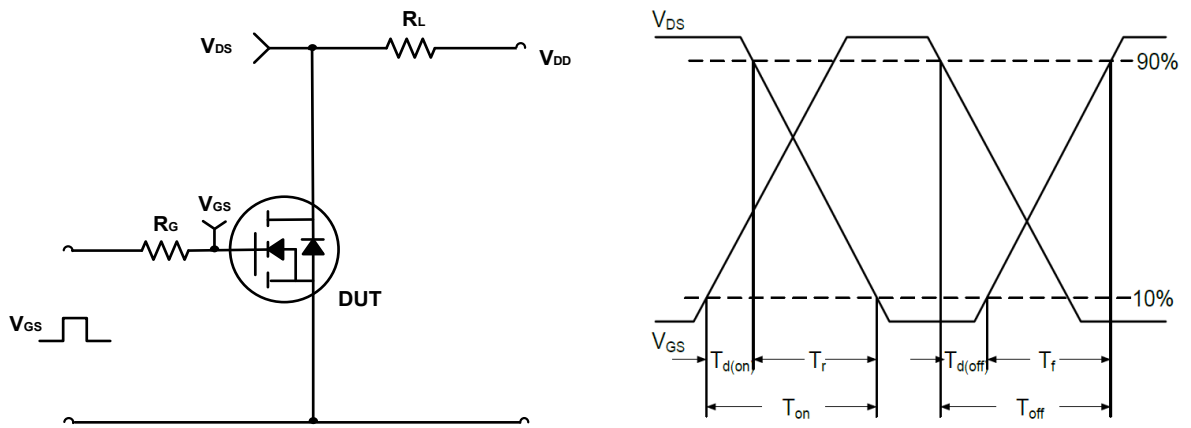


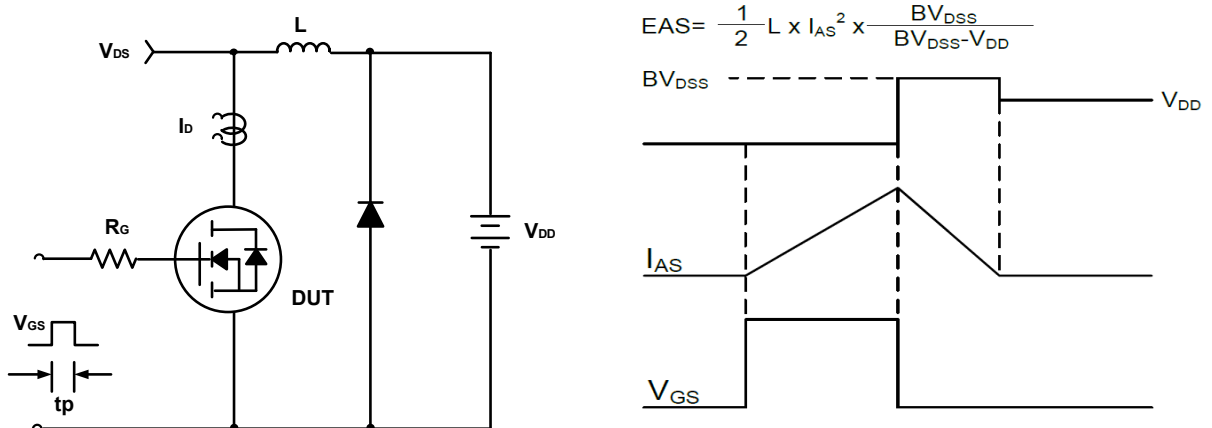
Figure 11. Normalized Maximum Transient Thermal Impedance



**Figure A. Gate Charge Test Circuit & Waveforms**

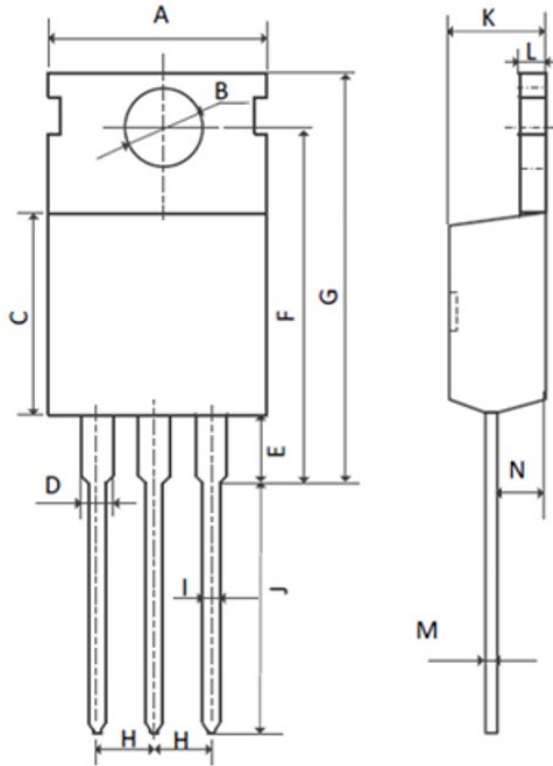


**Figure B. Switching Test Circuit & Waveforms**



**Figure C. Unclamped Inductive Switching Circuit & Waveforms**

COMMON DIMENSIONS



SYMBOL	MM	
	MIN	MAX
A	9.70	10.30
B	3.40	3.80
C	8.80	9.40
D	1.17	1.47
E	2.60	3.50
F	15.10	16.70
G	19.55MAX	
H	2.54REF	
I	0.70	0.95
J	9.35	11.00
K	4.30	4.77
L	1.20	1.45
M	0.40	0.65
N	2.20	2.60