

**General Description**

The MY008DNE5 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance.

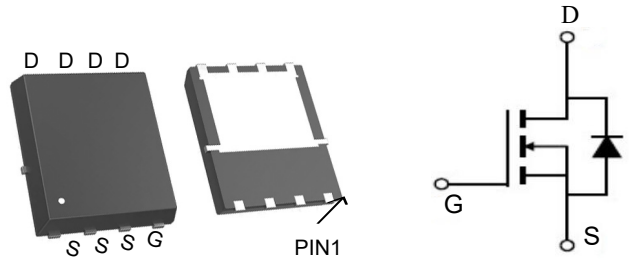


: YUhi fYg

$X_{FUU}$	40	X
$K$	60	C
$T_{FUQP} \cdot cXI U? 10X+$	>8	o á
$T_{FUQP} \cdot cXI U? 4.5X+$	>9.5	o á

**Application**

- Battery protection
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- W[ ě ě ] ě ě [ , ě ě ] ě



**DUW U[ Y A Uf ]b[ UbX CfXYf]b[ -bZfa U]cb**

DfcXi Wi-8	DUW	A Uf ]b[	E ImfD7 Gł
MY008DNE5	PDFN5*6-8L	MY008DNE5	5€€€

**5 Vgc`i ěY AU ja i a `FU]b[ g`fH,1&) °C unless otherwise noted)**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	60	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	26	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	8	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	100	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	31	mJ
$I_{AS}$	Avalanche Current	25	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	34.7	W
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>4</sup>	2	W
$T_s$ rn	Storage Temperature Range Operating	-55 to 150	°C
$T_J$	Junction Temperature Range	-55 to 150	°C
$R_{\theta JA}$	Thermal Resistance Junction-ambient (Steady State) <sup>1</sup>	62	°C/V
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	3.6	°C/J

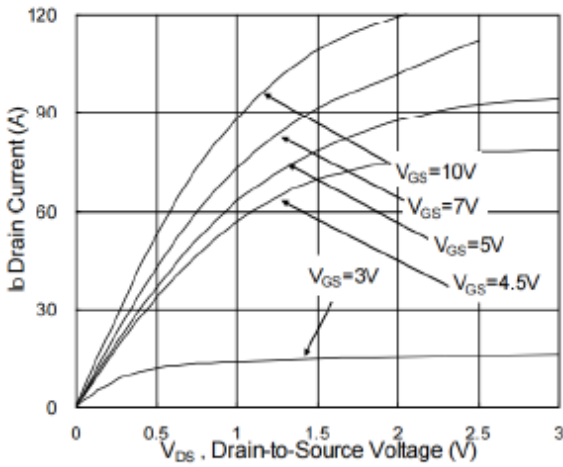
**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	40	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BVDSS Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	---	0.034	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	---	8.0	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	---	9.5	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250μA	1.0	1.5	2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-5.64	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	μA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	---	36	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	2.1	4.2	Ω
Q <sub>g</sub>	Total Gate Charge (4.5V)	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =12A	---	10.7	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	3.3	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	4.2	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =12V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3, I <sub>D</sub> =6A	---	8.6	---	ns
T <sub>r</sub>	Rise Time		---	3.4	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	25	---	
T <sub>f</sub>	Fall Time		---	2.2	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	1314	---	pF
C <sub>oss</sub>	Output Capacitance		---	120	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	88	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	42	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,5</sup>		---	---	100	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

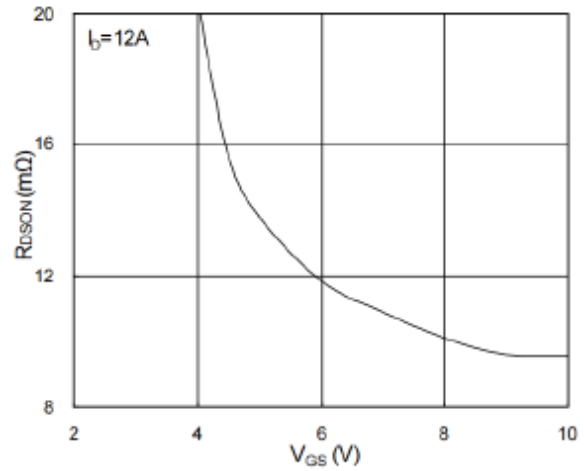
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup>FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=25V,V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=25A
- 4.The power dissipation is limited by 150°C junction temperature
- 5 . The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

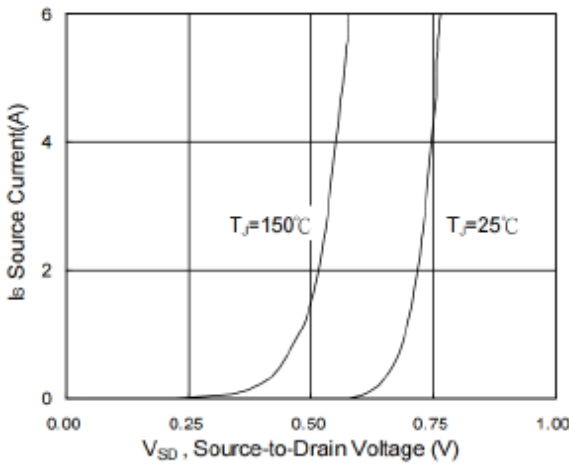
**Typical Characteristics**



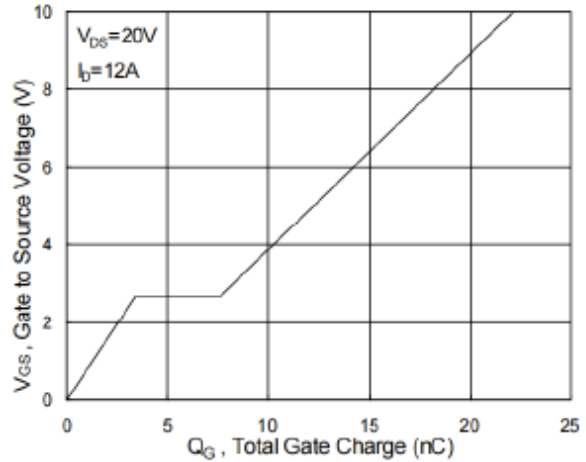
**Fig.1 Typical Output Characteristics**



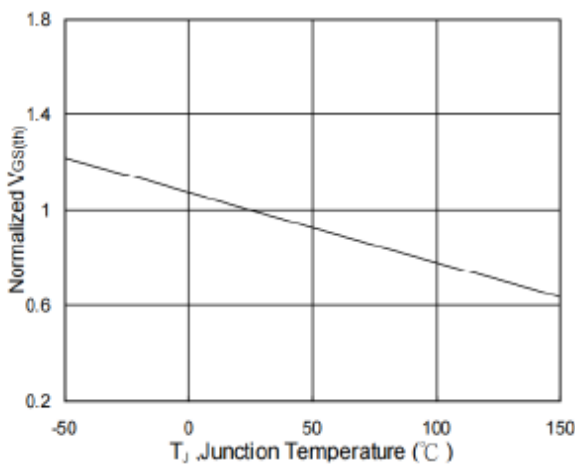
**Fig.2 On-Resistance vs. G-S Voltage**



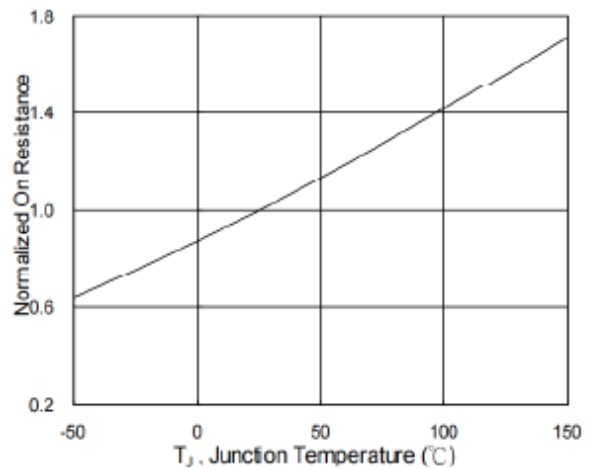
**Fig.3 Forward Characteristics of Reverse**



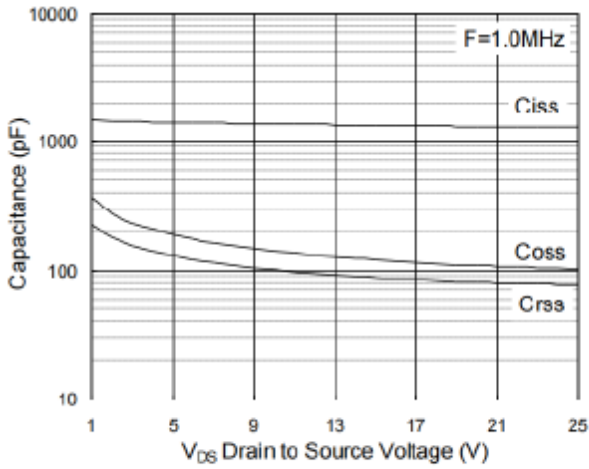
**Fig.4 Gate-Charge Characteristics**



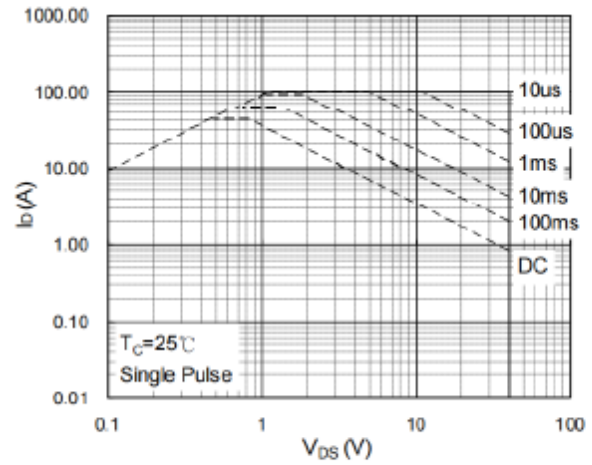
**Fig.5 V<sub>GS(th)</sub> vs. T<sub>J</sub>**



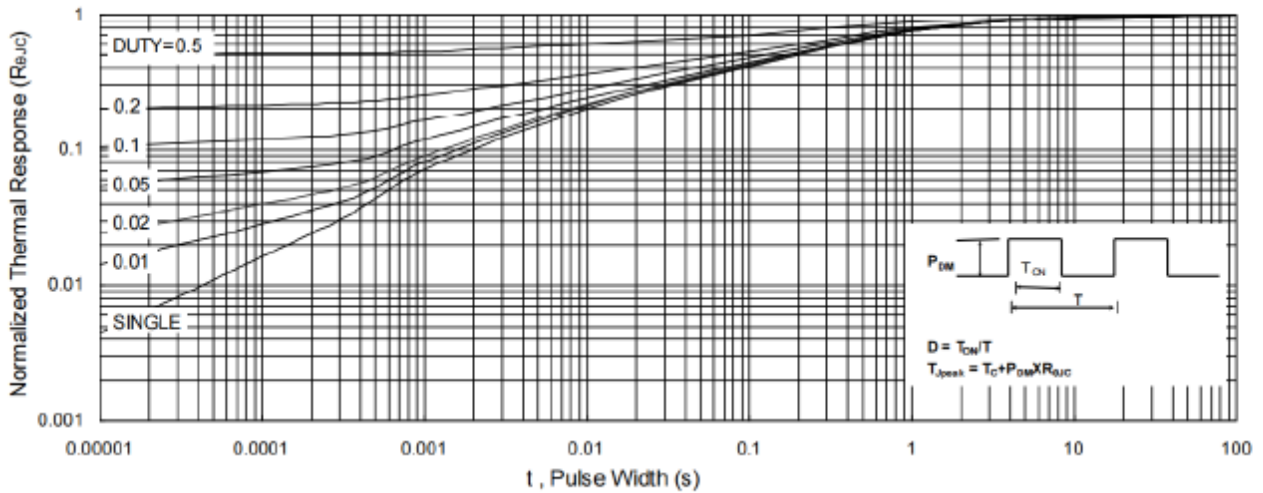
**Fig.6 Normalized R<sub>DS(on)</sub> vs. T<sub>J</sub>**



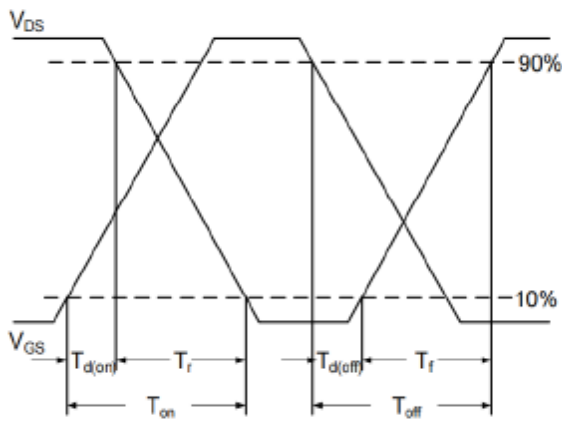
**Fig.7 Capacitance**



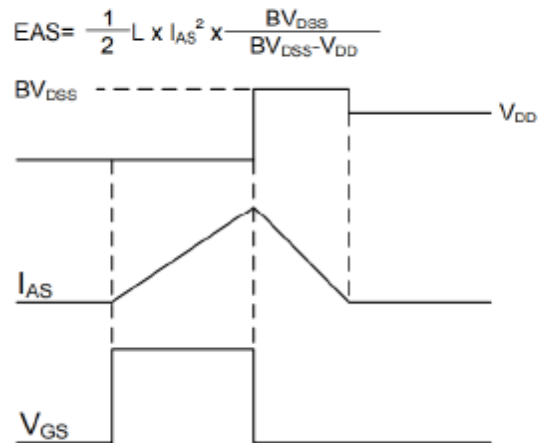
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

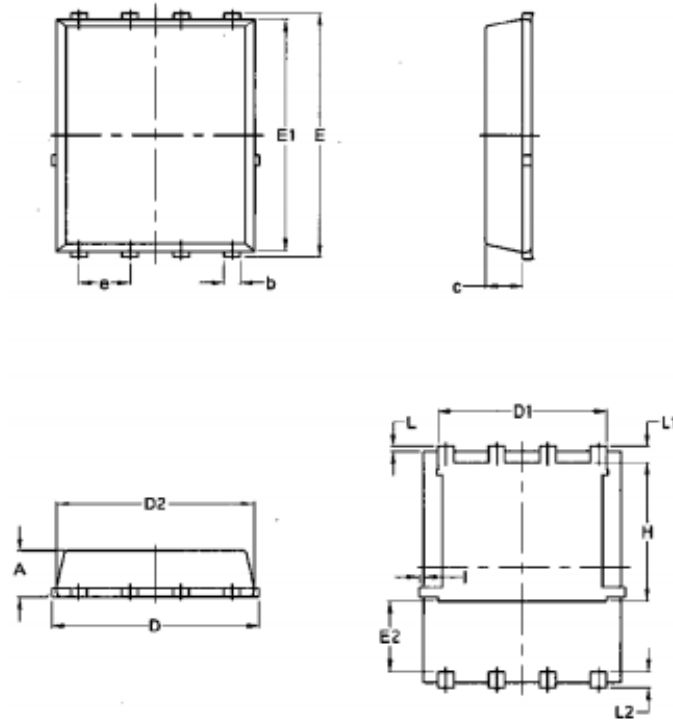


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**

**Package Mechanical Data-DFN5\*6-8L**



Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070