

## General Description

The IRFS3607TRPBF is silicon N-channel Enhanced VDMOSFETS, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

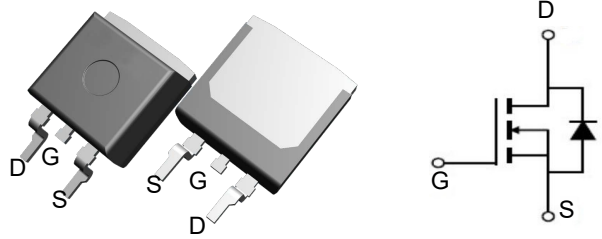


## Features

$V_{DSS}$	75	V
$I_D$	75	A
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$ )	7	$m\Omega$
$R_{DS(ON)}$ (at $V_{GS} = 10V$ )	10	$m\Omega$

## Application

- High efficiency switch mode power supplies
- Power factor correction
- Electronic lamp ballast



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
IRFS3607TRPBF	TO-263	IRFS3607TRPBF	2500

## Absolute Maximum Ratings ( $T_C=25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	75	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$T_C=25^\circ\text{C}$	80	A
	$T_C=100^\circ\text{C}$	75	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	245	
Continuous Drain Current	$T_A=25^\circ\text{C}$	13	A
	$T_A=70^\circ\text{C}$	10.5	
Avalanche Current <sup>C</sup>	$I_{AS}$	50	A
Avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AS}$	125	mJ
Power Dissipation <sup>B</sup>	$T_C=25^\circ\text{C}$	167	W
	$T_C=100^\circ\text{C}$	83	
Power Dissipation <sup>A</sup>	$T_A=25^\circ\text{C}$	2.1	W
	$T_A=70^\circ\text{C}$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ\text{C}$

**Electrical Characteristics (T<sub>c</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V	75			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			1 5	μA
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	3	4	V
I <sub>D(ON)</sub>	On state drain current	V <sub>GS</sub> =10V, V <sub>DS</sub> =5V	245			A
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =20A		7	8	mΩ
		TO220 T <sub>J</sub> =125°C		10	12	
		V <sub>GS</sub> =6V, I <sub>D</sub> =20A TO-220		6.1	7.9	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		60		S
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =1A, V <sub>GS</sub> =0V		0.7	1	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current <sup>G</sup>				70	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =40V, f=1MHz		3142		pF
C <sub>oss</sub>	Output Capacitance			435		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			43		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	0.6	1.3	2.0	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g(10V)</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =40V, I <sub>D</sub> =20A		44.5	63	nC
Q <sub>gs</sub>	Gate Source Charge			12		nC
Q <sub>gd</sub>	Gate Drain Charge			8		nC
t <sub>D(on)</sub>	Turn-On DelayTime	V <sub>GS</sub> =10V, V <sub>DS</sub> =40V, R <sub>L</sub> =2Ω, R <sub>GEN</sub> =3Ω		13.5		ns
t <sub>r</sub>	Turn-On Rise Time			11		ns
t <sub>D(off)</sub>	Turn-Off DelayTime			32		ns
t <sub>f</sub>	Turn-Off Fall Time			11		ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=500A/μs		29		ns
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =20A, dI/dt=500A/μs		161		nC

A. The value of R<sub>θJA</sub> is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25 °C. The Power dissipation P<sub>DSM</sub> is based on R<sub>θJA</sub> and the maximum allowed junction temperature of 150 °C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175 °C may be used if the PCB allows it.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=175 °C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=175 °C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25 °C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

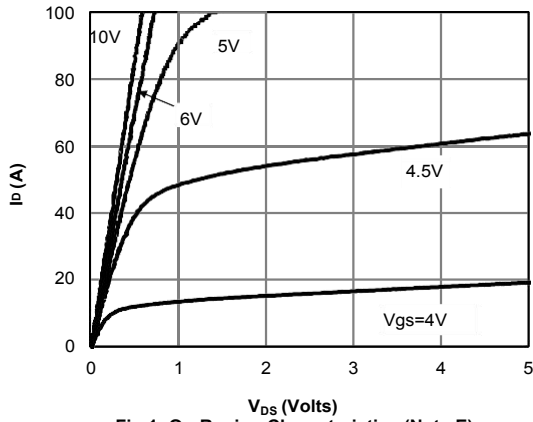
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=175 °C. The SOA curve provides a single pulse rating.

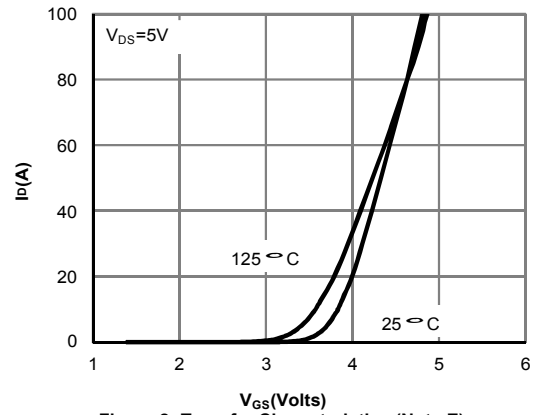
G. The maximum current limited by package.

H. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with T<sub>A</sub>=25 °C.

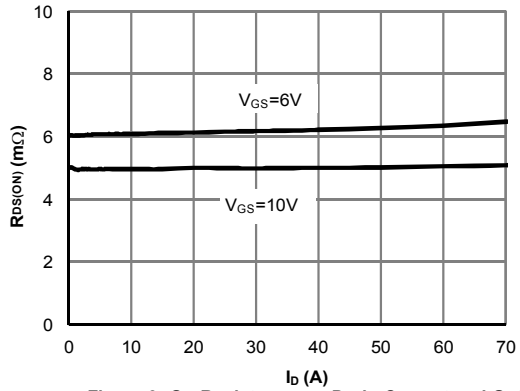
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



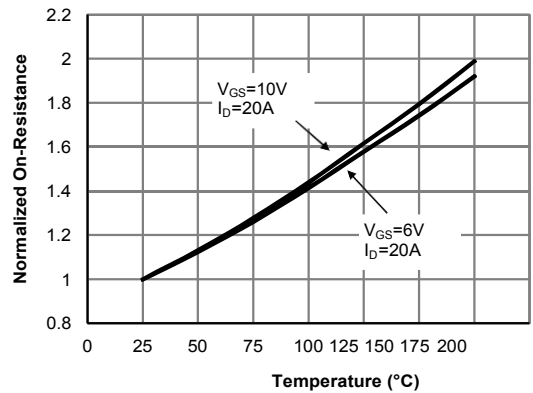
**Fig 1: On-Region Characteristics (Note E)**



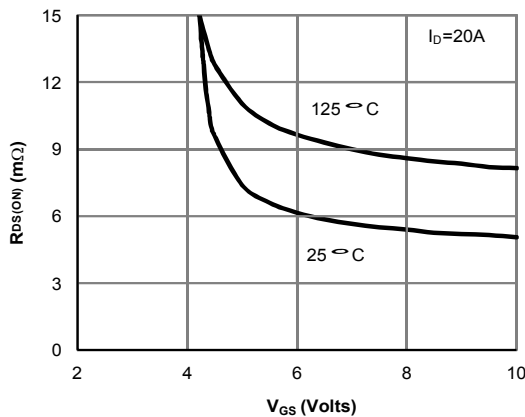
**Figure 2: Transfer Characteristics (Note E)**



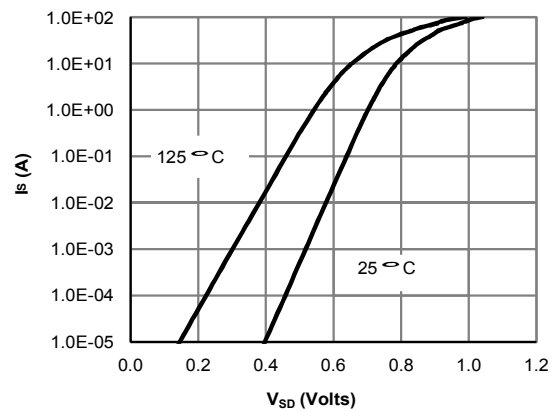
**Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)**



**Figure 4: On-Resistance vs. Junction Temperature (Note E)**



**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**



**Figure 6: Body-Diode Characteristics (Note E)**

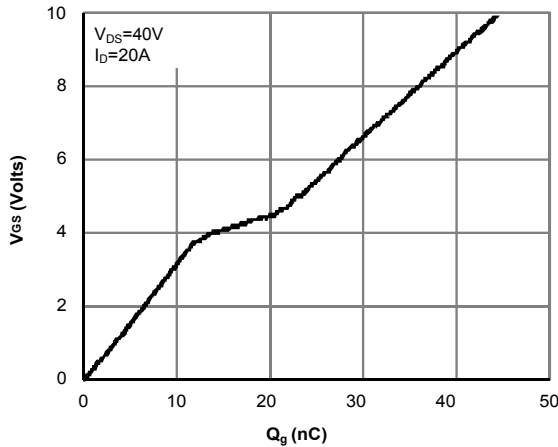


Figure 7: Gate-Charge Characteristics

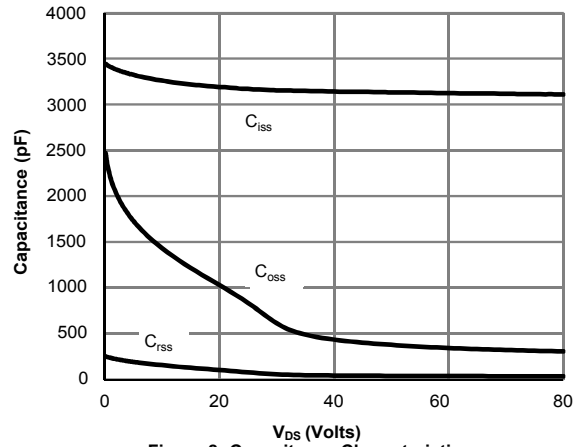


Figure 8: Capacitance Characteristics

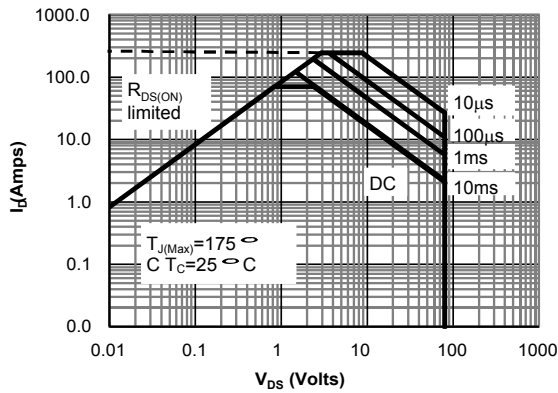


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

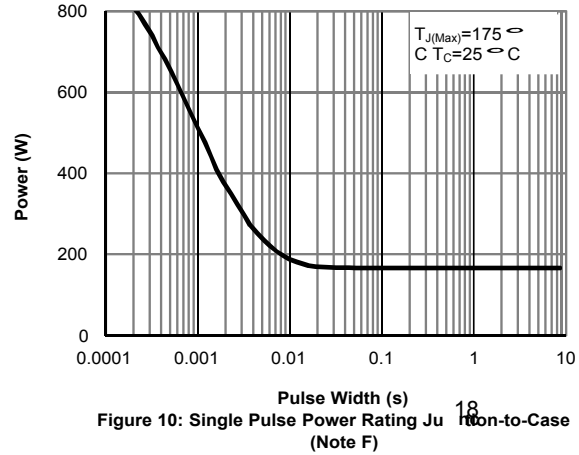


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

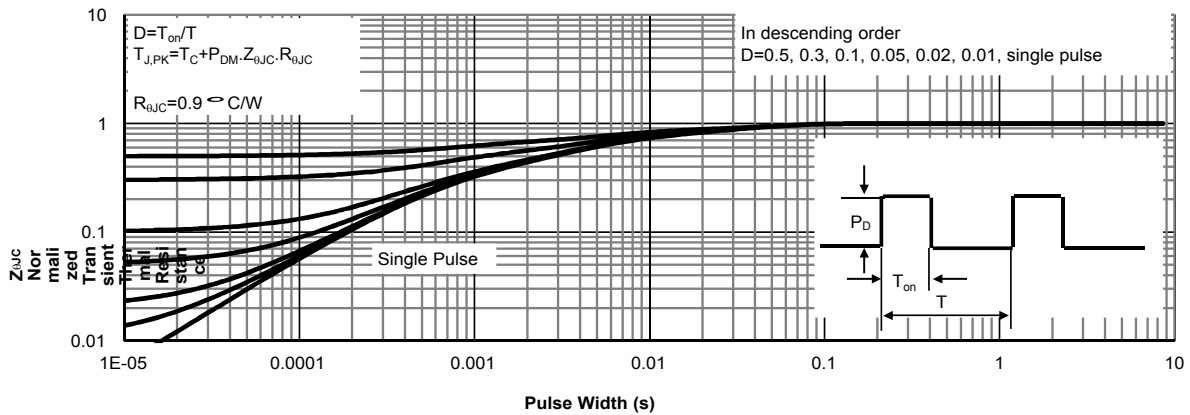


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

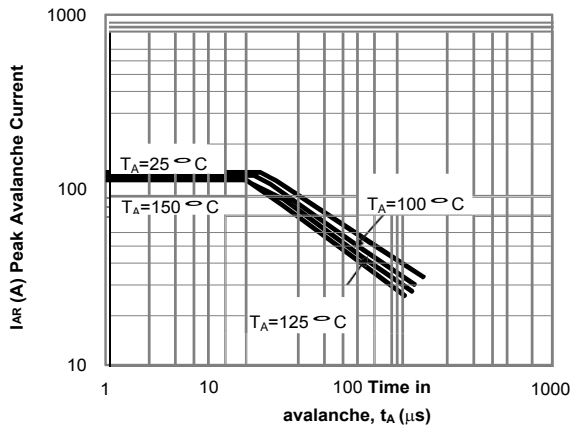


Figure 12: Single Pulse Avalanche capability (Note C)

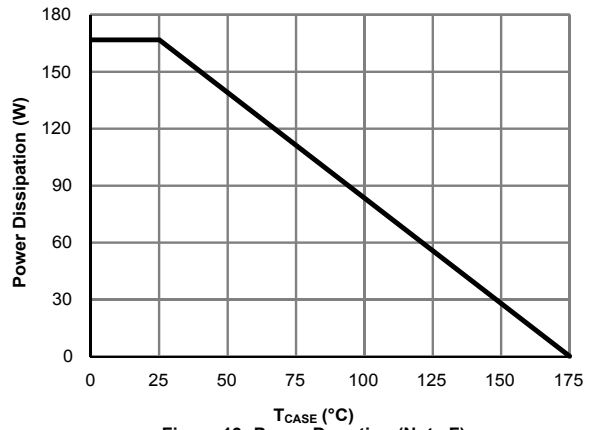


Figure 13: Power De-rating (Note F)

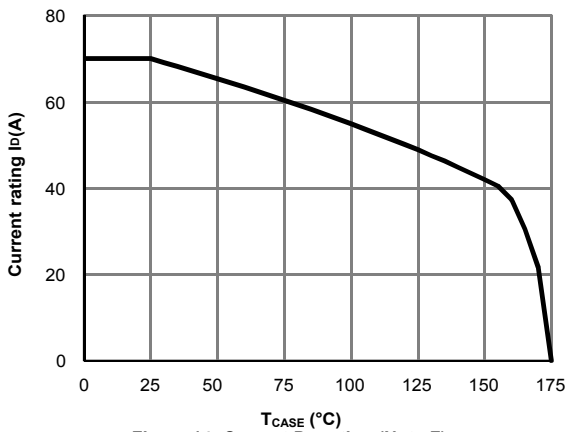


Figure 14: Current De-rating (Note F)

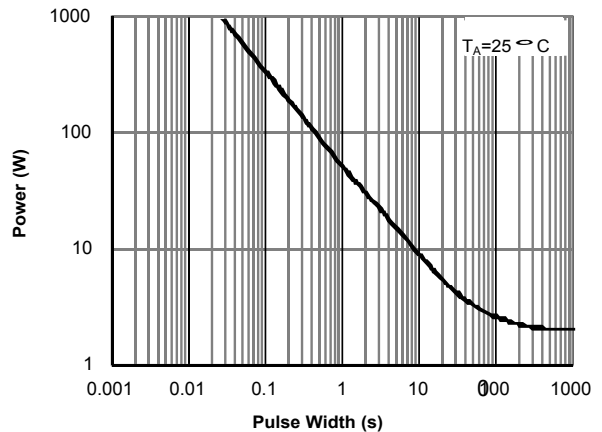


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

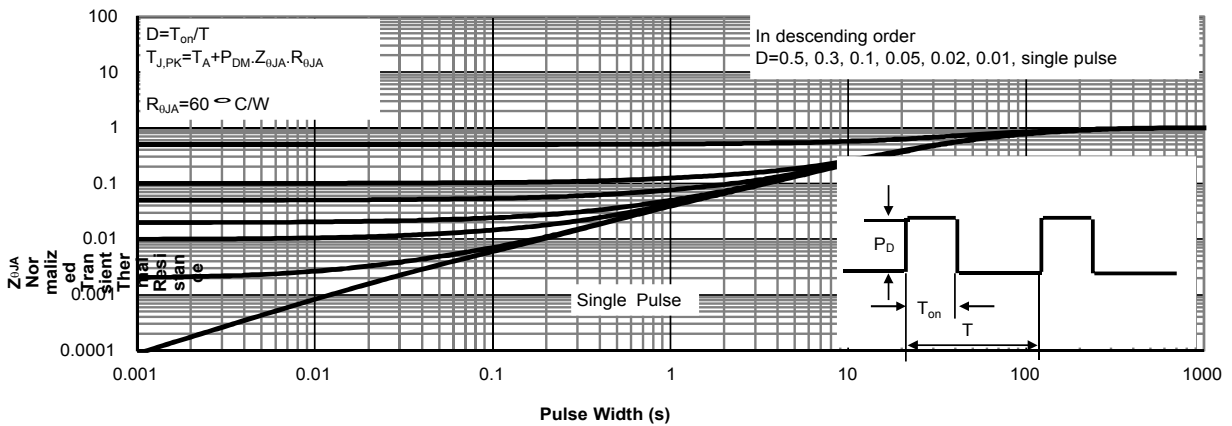
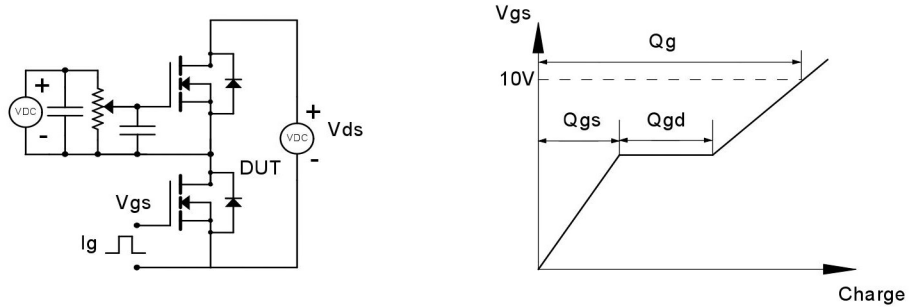
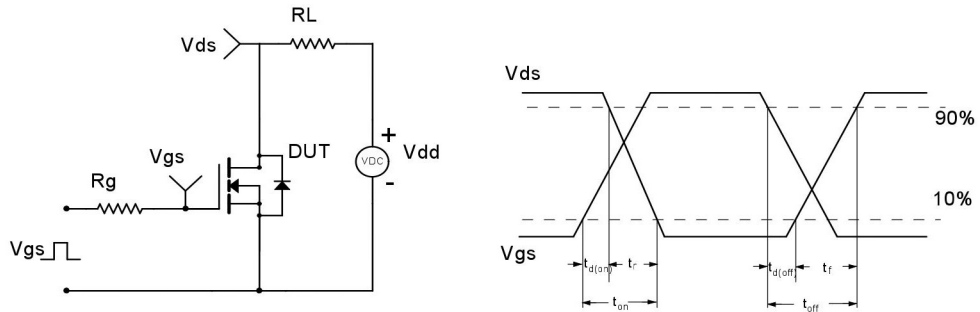


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

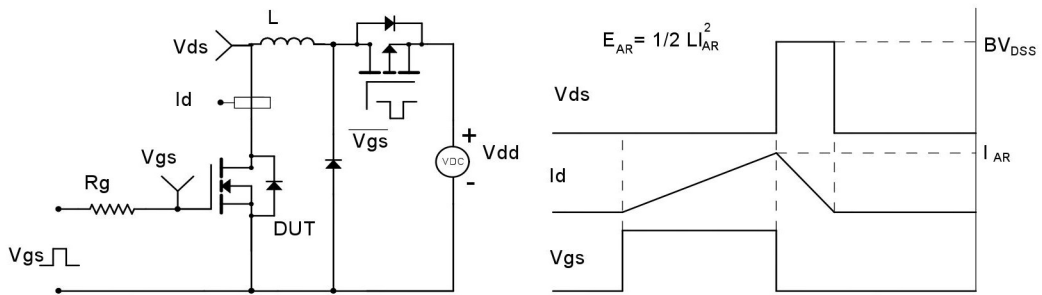
Gate Charge Test Circuit & Waveform



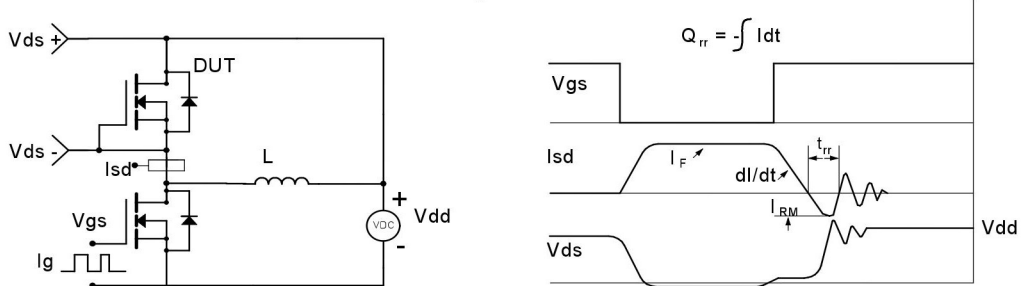
Resistive Switching Test Circuit & Waveforms



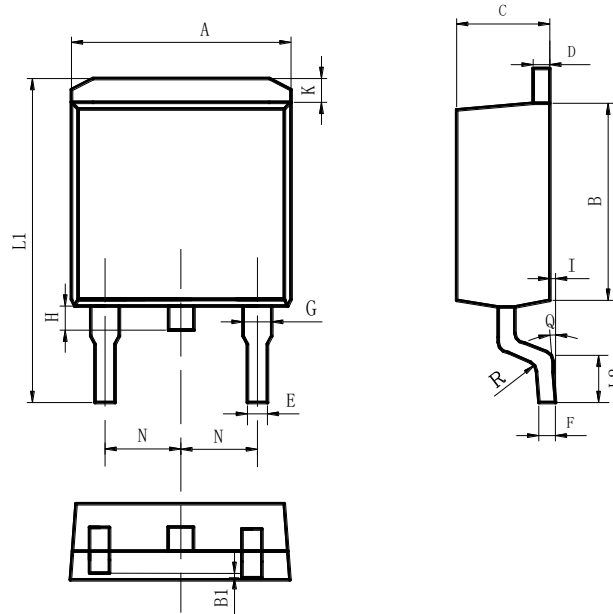
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



**Package Mechanical Data-TO-263 Single**



Items	Values(mm)	
	MIN	MAX
A	9.80	10.40
B	8.90	9.50
B1	0	0.10
C	4.40	4.80
D	1.16	1.37
E	0.70	0.95
F	0.30	0.60
G	1.07	1.47
H	1.30	1.80
K	0.95	1.37
L1	14.50	16.50
L2	1.90	2.90
I	0	0.2
Q	0°	8°
R	0.4	
N	2.39	2.69