## General Description

IRF840 the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

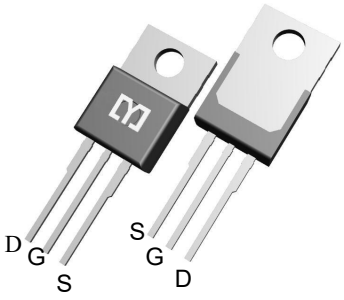
RoHS Compliant

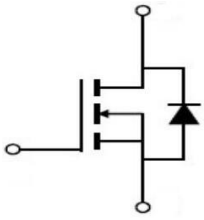
## Features

| | | |
|---|---|---|
| $V_{DSS}$ | 500 | V |
| $I_D$ | 10 | A |
| $P_D(T_C=25℃)$ | 50 | W |
| $R_{DS(ON)}(atV_{GS}=10V)$ | <0.7 | Ω |

## Application

- Battery protection
- Load switch
- Uninterruptible power supply



### Package Marking and Ordering Information

| Product ID | Pack | Marking | Qty(PCS) |
|---|---|---|---|
| IRF840 | TO-220 | IRF840 | 1000 |

### Absolute Maximum Ratings ($T_C$=25℃unless otherwise noted)

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 500 | V |
| $I_D$ | Drain Current | $T_j$=25℃ | 10.0 | A |
| | | $T_j$=100℃ | 5.7 | |
| $V_{GSS}$ | Gate-Source Voltage | | ±30 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy (note1) | | 190 | mJ |
| $I_{AR}$ | Avalanche Current (note2) | | 10.0 | A |
| $P_D$ | Power Dissipation (Tj=25℃) | | 50 | W |
| $T_j$ | Junction Temperature(Max) | | 150 | ℃ |
| $T_{stg}$ | Storage Temperature | | -55~+150 | ℃ |
| TL | Maximum lead temperature for soldering purpose,1/8" from case for 5 seconds | | 300 | ℃ |

## Thermal Characteristics

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance,Junction to Case | - | 1.88 | ℃/W |
| $R_{\theta JA}$ | Thermal Resistance,Junction to Ambient | - | 62.5 | ℃/W |

## Electrical Characteristics at $T_j$=25 ℃ unless otherwise specified

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Sourse Breakdown Voltage | ID=250μA, VGS=0 | 500 | -- | -- | V |
| $\triangle BV_{DSS}/\triangle T_J$ | Breakdown Voltage Temperature Conficient | $I_D$=250μA ,Reference to 25℃ | -- | 0.55 | -- | V/℃ |
| IDSS | Zero Gate Voltage Drain Current | Vds=500V, Vgs=0V | -- | -- | 1 | μA |
| | | Vds=400V, Tc=125℃ | | | 10 | μA |
| IGSSF | Gate-body leakage Current, Forward | Vgs=+30V, Vds=0V | -- | -- | 100 | nA |
| IGSSR | Gate-body leakage Current, | Vgs=-30V, Vds=0V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Date Threshold Voltage | Id=250uA,Vds=Vgs | 2 | -- | 4 | V |
| $R_{DS(on)}$ | Static Drain-Sourse | Id=4.5A,Vgs=10V | -- | 0.65 | 0.70 | Ω |
| **Dynamic Characteristics** | | | | | | |
| Ciss | Input Capacitance | VDS=25V，VGS=0，f=1.0MHz | -- | 1012 | -- | pF |
| Coss | Output Capacitance | | -- | 160 | -- | pF |
| Crss | Reverse Transfer Capacitance | | -- | 20 | -- | pF |
| **Switching Characteristics** | | | | | | |
| Td(on) | Turn-On Delay Time | VDD=250V，ID=10A，RG=25Ω (Note 3,4) | -- | 25 | 60 | nS |
| Tr | Turn-On Rise Time | | -- | 95 | 200 | nS |
| Td(off) | Turn-Off Delay Time | | -- | 55 | 120 | nS |
| Tf | Turn-Off Fall Time | | -- | 60 | 130 | nS |
| Qg | Total Gate Charge | VDS=400,VGS=10V， ID=10A (Note 3,4) | -- | 28 | 36 | nC |
| Qgs | Gate-Sourse Charge | | -- | 7 | -- | nC |
| Qgd | Gate-Drain Charge | | | 12.5 | -- | nC |
| **Drain-Sourse Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximun Continuous Drain-Sourse Diode Forward Current | | -- | -- | 9 | A |
| $I_{SM}$ | Maximun Plused Drain-Sourse DiodeForwad Current | | -- | -- | 36 | A |
| $V_{SD}$ | Drain-Sourse Diode Forward | Id=10A | -- | -- | 1.45 | V |
| trr | Reverse Recovery Time | $I_S$=10.0A,$V_{GS}$ =0V $di_F/dt$=100A/μs (Note3) | -- | 300 | -- | nS |
| Qrr | Reverse Recovery Charge | | -- | 2.2 | -- | μC |

*Notes 1, L=8mH, IAS=10 A,VDD=50V, RG=25Ω, Starting TJ =25°C

2, Repetitive Rating : Pulse width limited by maximum junction temperature

3, Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%

4, Essentially Independent of Operating Temperature

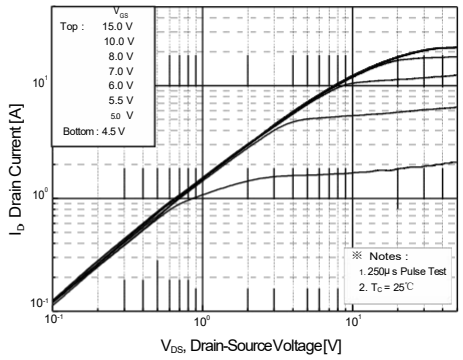



**Figure 1. On-Region Characteristics**

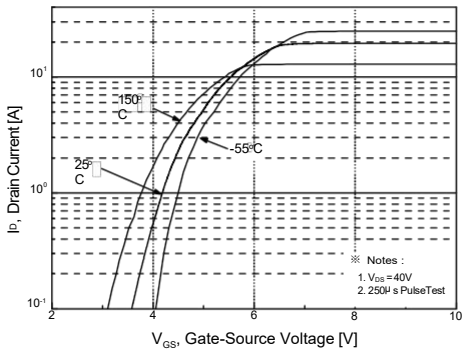



**Figure 2. Transfer Characteristics**

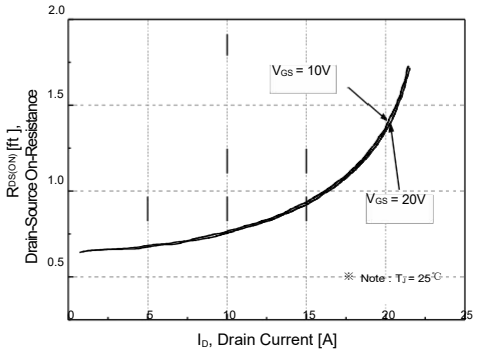



**Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage**

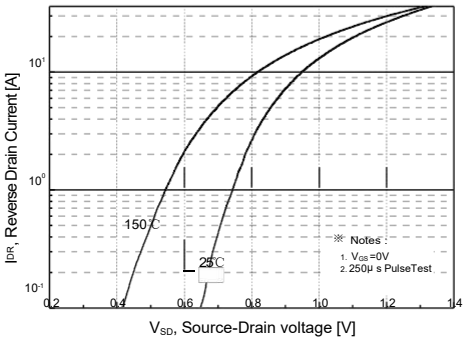



**Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature**

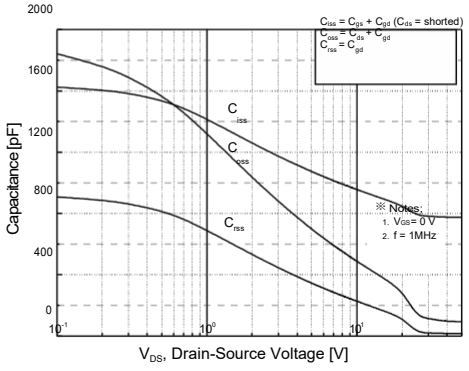



**Figure 5. Capacitance Characteristics**

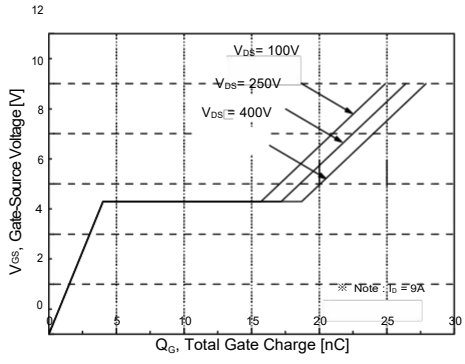



**Figure 6. Gate Charge Characteristics**

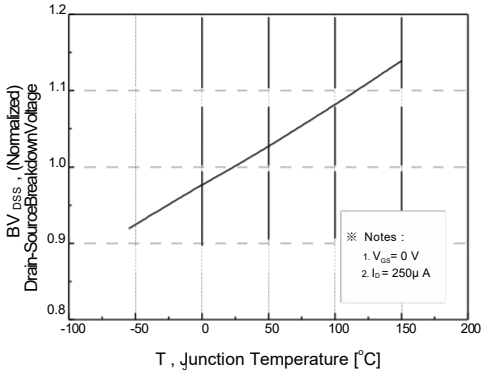



**Figure 7. Breakdown Voltage Variation vs Temperature**

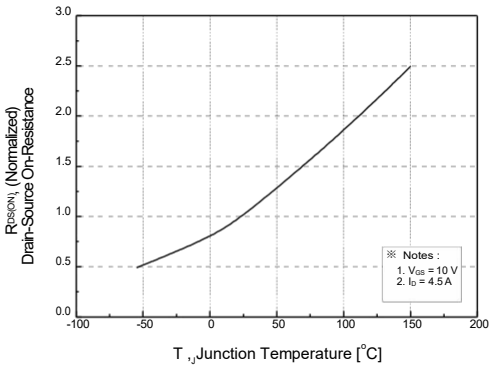



**Figure 8. On-Resistance Variation vs Temperature**

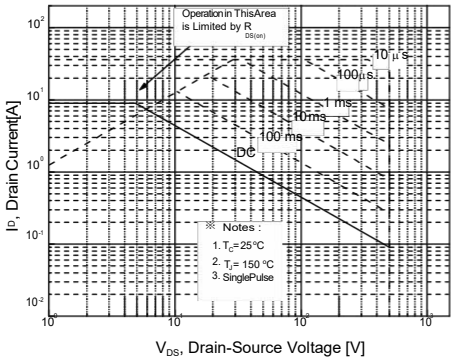



**Figure 9-2. Maximum Safe Operating Area**

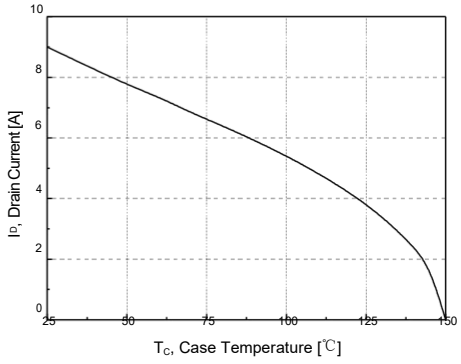



**Figure 10. Maximum Drain Current vs Case Temperature**

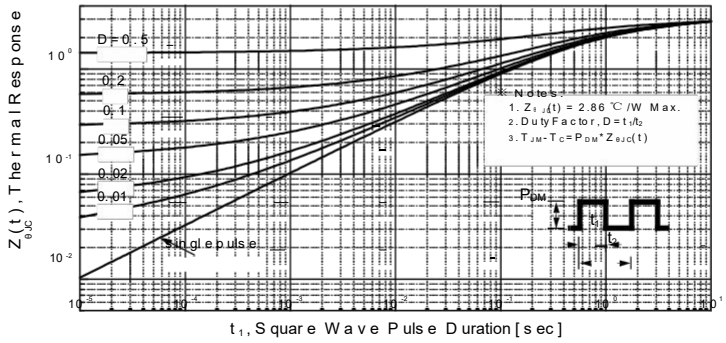
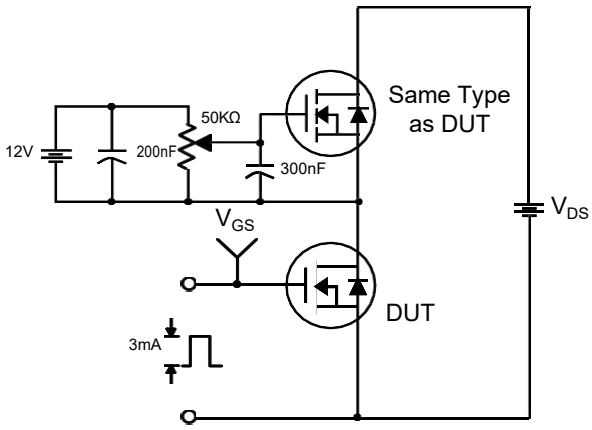
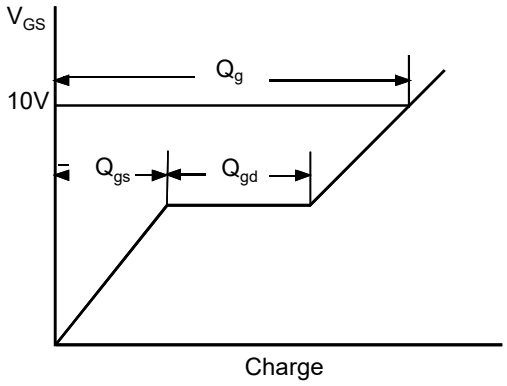


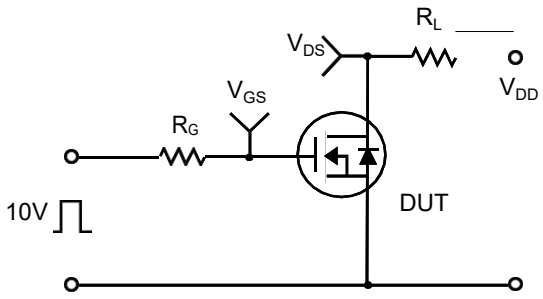

**Figure 11-2. Transient Thermal Response Curve**

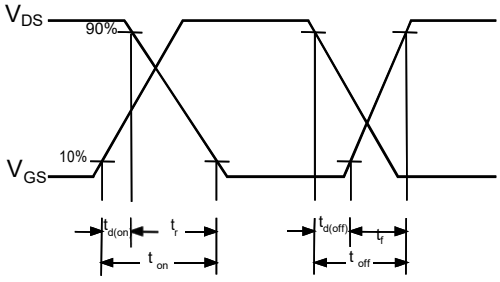
### Gate Charge Test Circuit & Waveform



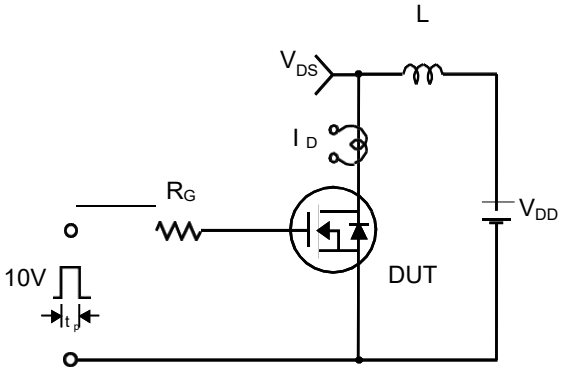




### Resistive Switching Test Circuit & Waveforms

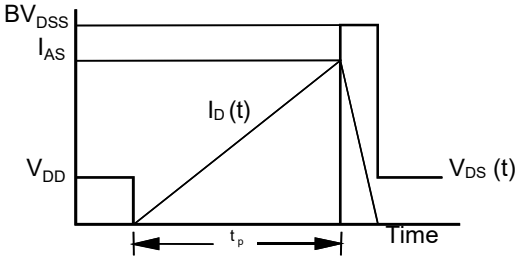


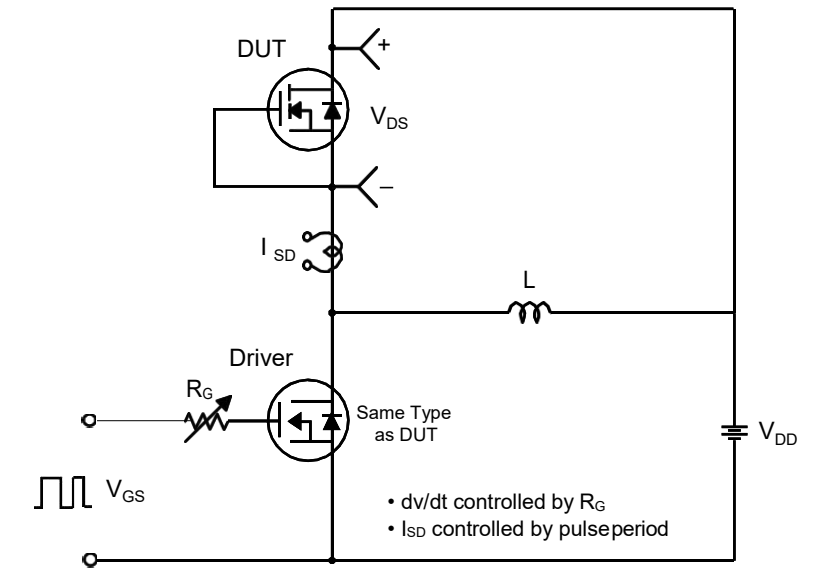

### Unclamped Inductive Switching Test Circuit & Waveforms

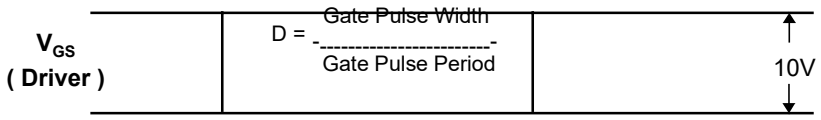


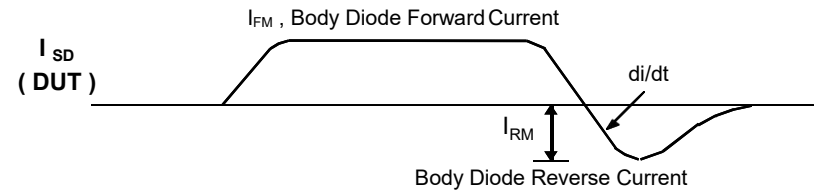

$$E_{AS} = \frac{1}{2} LI^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

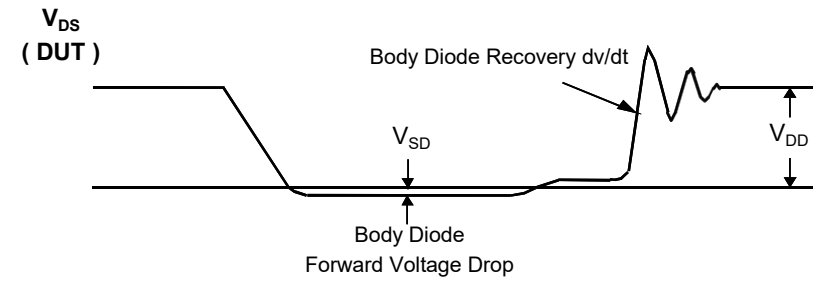


**Peak Diode Recovery dv/dt Test Circuit & Waveforms**

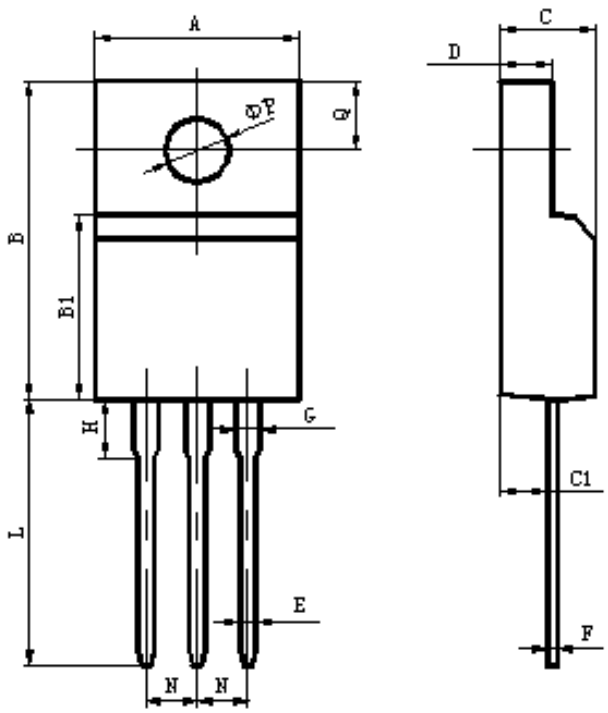


## Package Mechanical Data-TO-220 Single




| Items | Values(mm) | |
|---|---|---|
| | MIN | MAX |
| A | 9.60 | 10.4 |
| B | 15.4 | 16.2 |
| B1 | 8.90 | 9.50 |
| C | 4.30 | 4.90 |
| C1 | 2.10 | 3.00 |
| D | 2.40 | 3.00 |
| E | 0.60 | 1.00 |
| F | 0.30 | 0.60 |
| G | 1.12 | 1.42 |
| H | 3.40 | 3.80 |
| | 2.40 | 2.90 |
| L* | 12.0 | 14.0 |
| N | 2.34 | 2.74 |
| Q | 3.15 | 3.55 |
| Φ P | 2.90 | 3.30 |