8205A

20V Dual N-Channel Enhancement Mode MOSFET

MAOYUAN semiconductor

General Description

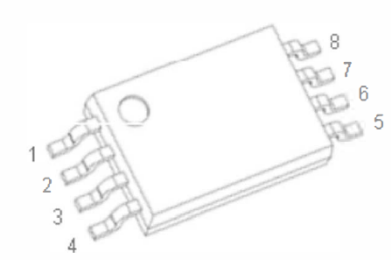
The 8205A is the low RDSON trenched N-CH MOSFETS with robust ESD protection. This product is suitable for Lithium-ion battery pack applications.

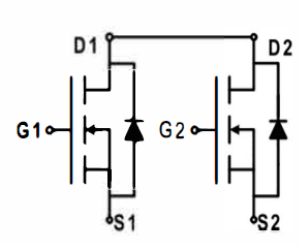
Features

V_{DSS}	20	V
I_D	7	A
$R_{DS(ON)}$(atV_{GS}=10V)	11	mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	15	mΩ

Application

- Green Device Available
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Advanced high cell density Trench technology





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
8205A	TSSOP-8	8205A	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±10	V
I_D	Continuous Drain Current	T_A=25℃	7.0	A
		T_A= 100℃	4.5	A
I_{DM}	Pulsed Drain Current note1		24	A
P_D	Power Dissipation	T_A= 25℃	1.23	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		111	℃/W
T_J T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20			V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V , I_D=3.5A V_{GS}=2.5V , I_D=3.5A		11 15	15 18	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	0.5		1.2	V
I_{DSS}	Drain-Source Leakage Current	V_{DS}=16V , V_{GS}=0V , T_J=25℃			1	uA
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±8V , V_{DS}=0V			±100	nA
gfs	Forward Transconductance	V_{DS}=5V , I_D=3.5A		20		S
Q_g	Total Gate Charge (4.5V)			11.3		
Q_{gs}	Gate-Source Charge	V_{DS}=15V , V_{GS}=4.5V , I_D=7A		1.89		nC
Q_{gd}	Gate-D rain Charge			3.56		
$T_{d(on)}$	Turn-On Delay Time			8		
T_r	Rise Time	V_{DD}=10V , V_{GS}=4.5V , R_G=3.3Ω		17		ns
$T_{d(off)}$	Turn-Off Delay Time	I_D=3.5A		27		
T_f	Fall Time			8.8		
C_{iss}	Input Capacitance			955		
C_{oss}	Output Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz		200		pF
C_{rss}	Reverse Transfer Capacitance			150		

Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

Figure1: Output Characteristics

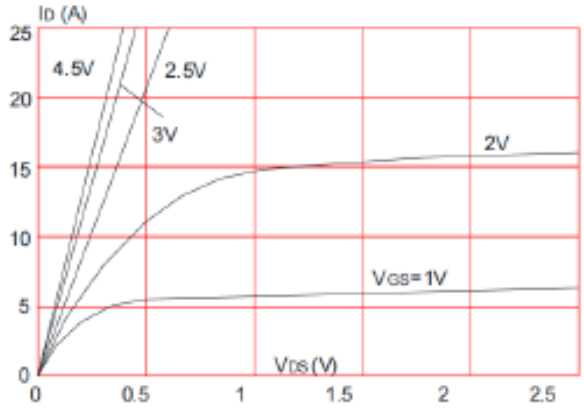


Figure 2: Typical Transfer Characteristics

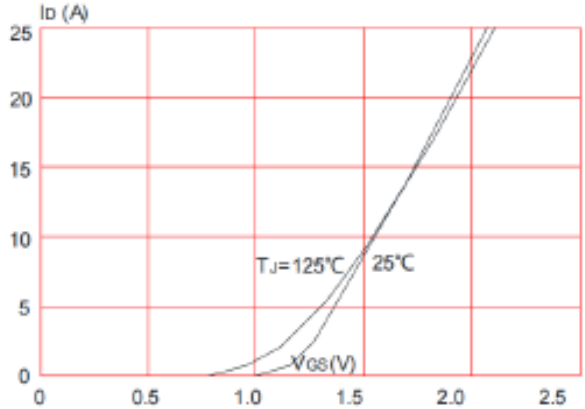


Figure 3: On-resistance vs. Drain Current

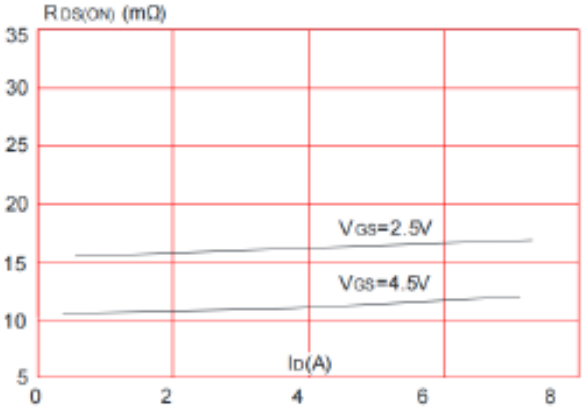


Figure 4: Body Diode Characteristics

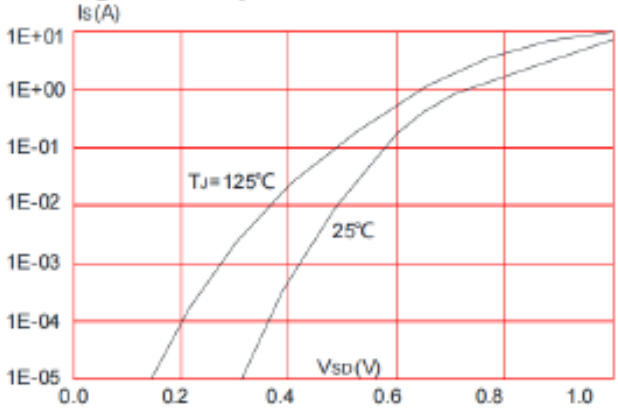


Figure 5: Gate Charge Characteristics

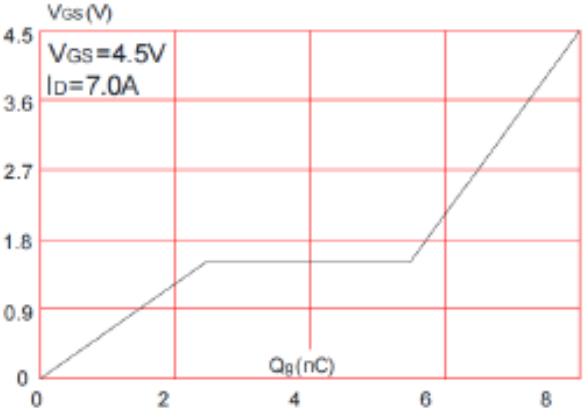


Figure 6: Capacitance Characteristics

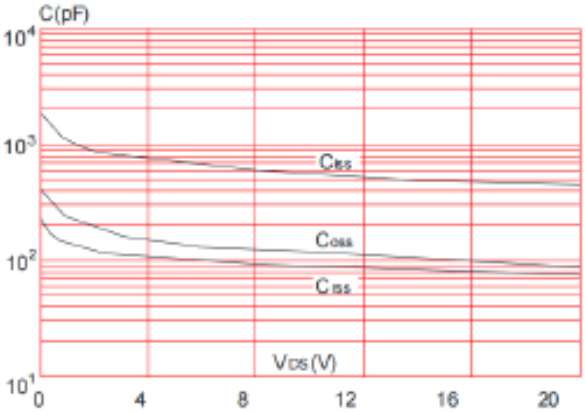


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

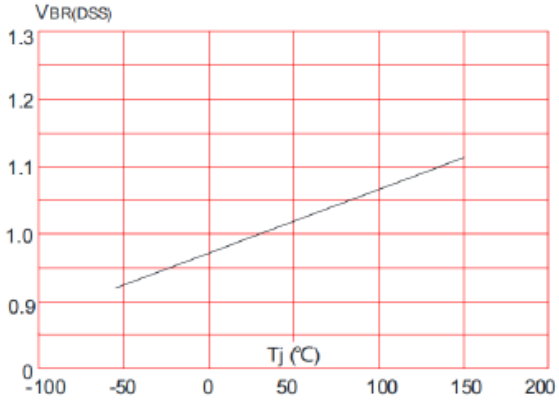


Figure 8: Normalized on Resistance vs. Junction Temperature

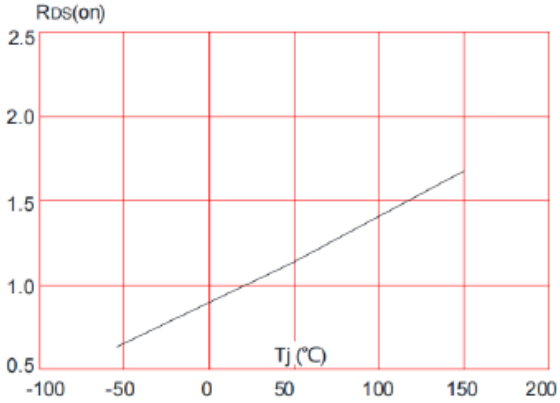


Figure 9: Maximum Safe Operating Area

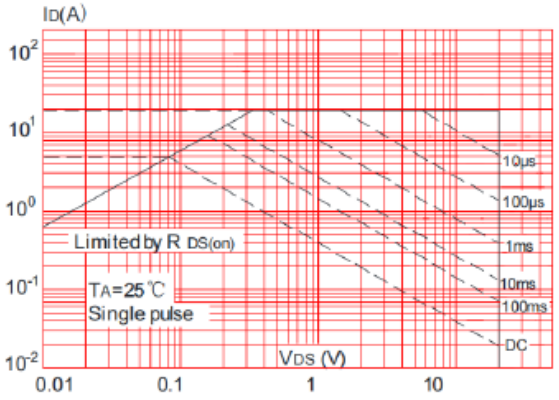


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

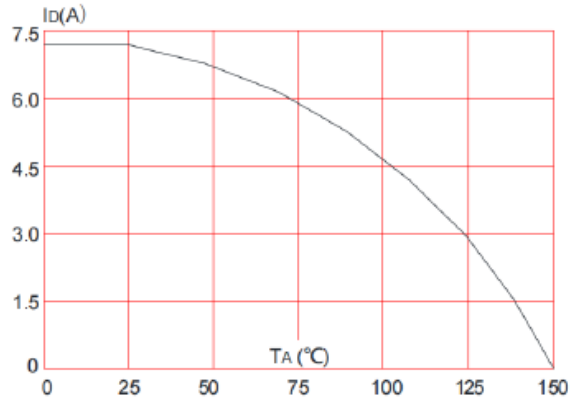
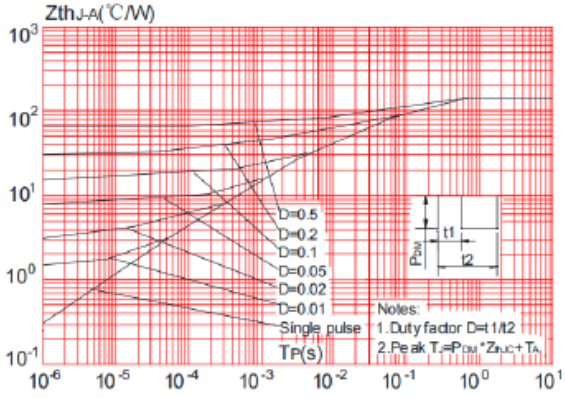
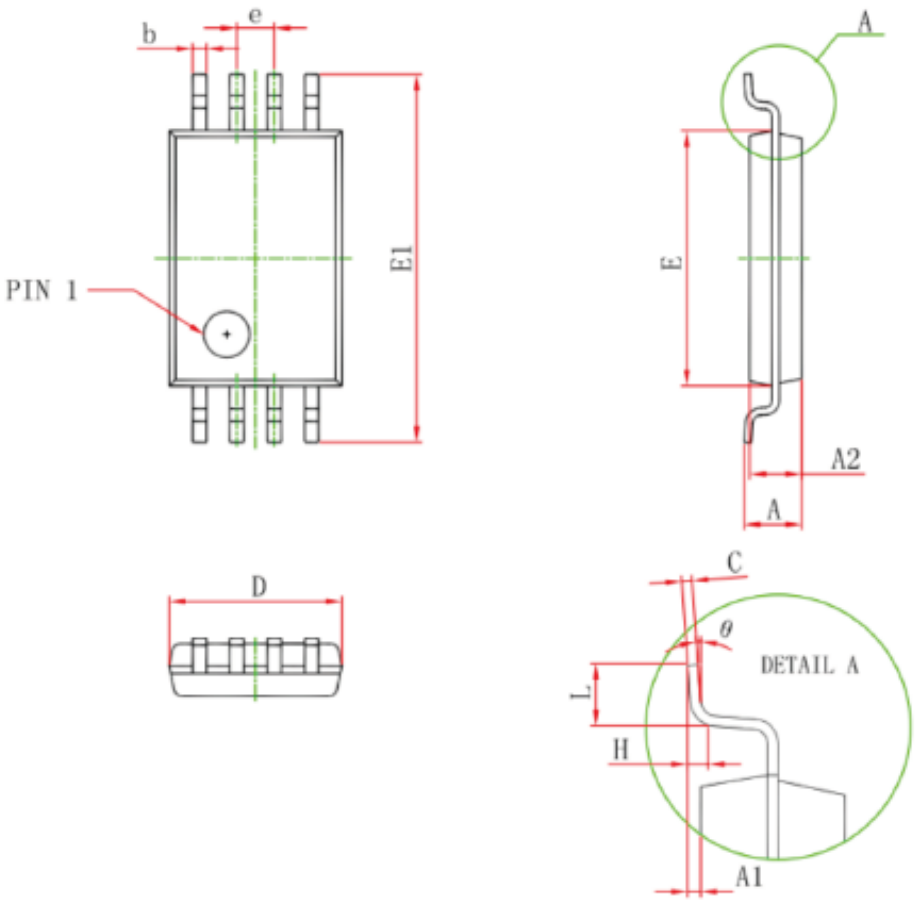


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Package Mechanical Data-TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°